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FOREIGN TECHNOLOGY DIVISION

DESIGN OF DIGITAL CONTROL SYSTEMS
(Selected Portions)

by

V. P. Petrov

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EDITED MACHINE TRANSLATION

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By: V. P. Petrov

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(U) This book is intended for personnel working in the field of instrument engineering and in the application of discrete electronic elements for the automation and control of various industrial processes. The book deals with problems of designing equipment for automatic control systems consisting of decentralized objects. Functional-assembly methods of designing various-purpose electronic equipment through the use of standard high-reliability electronic elements are described. A number of standard elements and structures are recommended for wide application in the development of digital computer devices, equipment, units of industrial automation, computing technique, control, communication, and signaling. Methods for the optimization (minimization) of switching circuits are discussed. A multi-purpose telemetric-computing system, suitable for industrial production, dispatching, automatic control of irrigation installations, oil wells, water and gas distribution systems, etc., is described. Also discussed are engineering calculations for reliability and noise immunity of data transmission systems and technical and economic efficiency in the designing of electronic equipment for automatic control systems. No personalities are mentioned. There are 50 Soviet and 8 non-Soviet references.

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U. S. BOARD ON GEOGRAPHIC NAMES TRANSLITERATION SYSTEM

Block	Italic	Transliteration	Block	Italic	Transliteration
А а	*А а*	A, a	Р р	*Р р*	R, r
Б б	*Б б*	B, b	С с	*С с*	S, s
В в	*В в*	V, v	Т т	*Т т*	T, t
Г г	*Г г*	G, g	У у	*У у*	U, u
Д д	*Д д*	D, d	Ф ф	*Ф ф*	F, f
Е е	*Е е*	Ye, ye; E, e*	Х х	*Х х*	Kh, kh
Ж ж	*Ж ж*	Zh, zh	Ц ц	*Ц ц*	Ts, ts
З з	*З з*	Z, z	Ч ч	*Ч ч*	Ch, ch
И и	*И и*	I, i	Ш ш	*Ш ш*	Sh, sh
Й й	*Й й*	Y, y	Щ щ	*Щ щ*	Shch, shch
К к	*К к*	K, k	Ъ ъ	*Ъ ъ*	"
Л л	*Л л*	L, l	Ы ы	*Ы ы*	Y, y
М м	*М м*	M, m	Ь ь	*Ь ь*	'
Н н	*Н н*	N, n	Э э	*Э э*	E, e
О о	*О о*	O, o	Ю ю	*Ю ю*	Yu, yu
П п	*П п*	P, p	Я я	*Я я*	Ya, ya

* ye initially, after vowels, and after ъ, ь; e elsewhere. When written as ё in Russian, transliterate as yё or ё. The use of diacritical marks is preferred, but such marks may be omitted when expediency dictates.

DESIGN OF DIGITAL CONTROL SYSTEMS

V. P. Petrov

5.5 Complex of Pulse FT Elements for 200 kHz

A complex of ferrite-transistor elements [FT] (ФТ) is intended for construction of general-purpose control computers and devices of discrete automation working in the frequency range up to 200 kHz.

All the modulus of the complex are powered from a stabilized 12.6 V ±10%.

The modules keep their efficiency with ambient temperature variation from -10°C to +50°C, and at an atmospheric humidity of 95-98% at an ambient temperature of +40°C; at vibration loads in the frequency range 10-70 Hz with acceleration up to 3.5 g; at impact loads with 100-120 g acceleration.

The load capacity of the elements is low – 3-4 elements. The complex has six modules having the original diagram of construction.

Module FT-1

This module is a universal low-capacity logic element fulfilling the following operations:

a) storage of input information;

b) inhibition of input information;

c) collection of information on two inputs.

The module is built according to the schematic diagram shown in Fig. 51. Signals proceeding to the "Record" winding are recorded by transformer [Tr_1] (Tp_1), consisting of core 0.25 [VT] (BT) (K-272) K2 × 1.4 × 0.8. During readout of information on the "Cycle" or "Inhibit" winding, triode T of the module is opened by the emf induced on base winding of the core of Tr_1. The base winding has two sections 6 and 7, which permits obtaining the nominal and expanded width of the output pulse. The characteristic peculiarity is the introduction of a second transformer Tr_2 (core M 2000-[NM] (HM)-1, K7 × 4 × 2), carrying out positive feedback between output and base currents.

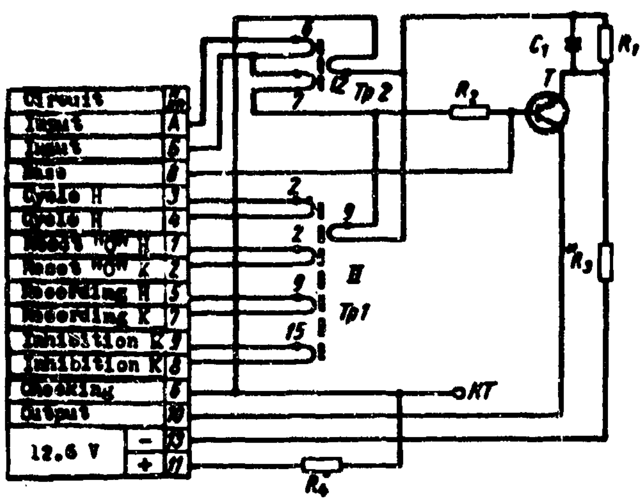


Fig. 51. Schematic diagram of FT-1.

Circuit elements R_1 and R_3 realize reverse bias of the emitter junction. Circuit R_1C_1 shapes pulse width. Resistors R_2 and R_4 limit base and collector currents, respectively.

The power consumed by the module at the maximum working frequency and under normal working conditions without load in the output circuit is equal to 0.4 W with the nominal width of output signal and 0.6 W with the expanded width of output signal.

Constructively the module is shaped on a separate laminated insulation plate and measures not more than 54 x 34 x 21 mm. The weight of the module is 15 g.

Module FT-2

The module is a universal powerful logic element fulfilling the operations:

a) storage of input information;

b) inhibition of input information.

The schematic diagram of the module shown in Fig. 52 contains three transformers, Tr_1, Tr_2, and Tr_3, consisting of cores 0.25 VT (K-272) K2 x 1.4 x 0.8.

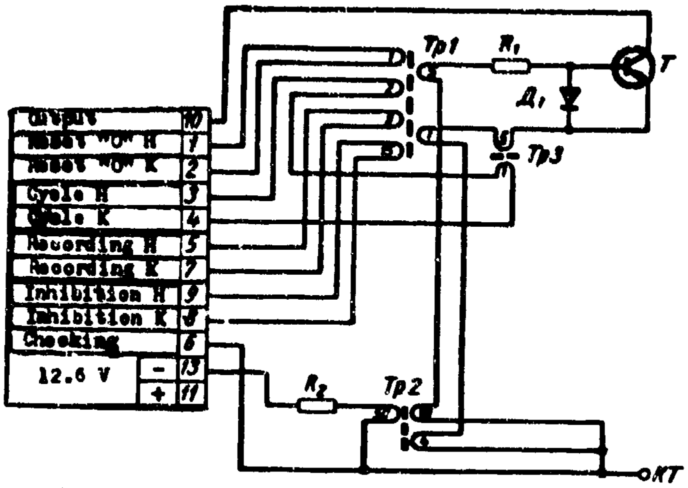


Fig. 52. Schematic diagram of module FT-2.

During readout of information recorded in Tr_1, on the "Cycle" winding triode T is opened by the emf induced on the base winding.

The emitter current of the triode magnetizes the core of Tr_2 in the direction opposite to that in which it has been magnetized up to this point. The induced emf on the base winding of Tr_2 puts the triode into deep saturation.

Under the action of displacement current flowing in the winding, the core of transformer Tr_2 returns to its initial state. Resistor R_2 determines the value of this current. Diode $Д_1$ protects the emitter junction of the triode, and resistor R_1 limits the current of the triode base. The limitation of the collector current and the compensation of interference appearing at the time of the entrance of cycle pulses in the absence of information on the core of Tr_1 is carried out by transformer Tr_3. The power consumed by module FT-2 in conjunction with FT-6 at maximum working frequency under normal working conditions without load in the output circuit is equal to 2.4 W.

The electrical, load, and reliability characteristics of the module are given in Table 50.

Constructively the module is shaped in the form of a separate plate measuring 54 × 35 × 24 mm. The weight of the module is not more than 55 g.

Table 50.

Type of cell	Amplitude of input signal				Parameters of input signal without load in output circuit			
	"Recording" in mA	"Inhibition" in mA	"Cycle" A in mA	"Reset" A in mA	Amplitude of output current in mA	Width of output pulses: Normal in μs	Width of output pulses: Expanded in μs	Width of front in μs
ФТ-1	65—150	65—150	1,0—1,5	1,0—1,5	95—135	1,1—1,6	1,5—2,2	0,15—0,6
ФТ-2	65—150	65—150	1,0—1,5	1,0—1,5	1,0—1,2	1,2—1,6	—	0,3—0,6
ФТ-3	65—150	65—150	1,0—1,5	1,0—1,5	1,0—1,5	—	3,2—6	0,2—0,7
ФТ-4	65—150	—	—	—	70—95	1,4—2,0, delay time 0,025 μs	—	—
ФТ-5	65—150	—	1,0—1,5	—	90—130	1,8—2,4	—	0,4—0,9
ФТ-6	—	—	—	—	—	—	—	—

Table [illegible]. (Cont'd)

Type of cell	Maximum working frequency	Noise immunity on "Record" winding	Load capacity					Failure rate in 1/h
			ФТ-1	ФТ-2	ФТ-3	ФТ-4	ФТ-5	
ФТ-1	200	10	—	9/6	—	9/6	9/6	$1 \cdot 10^{-6}$
ФТ-2	200	10	—	20	—	—	12	$1 \cdot 10^{-6}$
ФТ-3	25	10	—	—	20 (30 "Inhibition")	15	15	$1 \cdot 10^{-6}$
ФТ-4	200	12	3	—	—	3	1	$2 \cdot 10^{-6}$
ФТ-5	200	20	—	—	4	3	2	$1 \cdot 10^{-6}$
ФТ-6	—	—	—	—	—	—	—	$0{,}4 \cdot 10^{-6}$

Module FT-3

This is a powerful extinguishing pulse amplifier. With the help of the module it is possible to carry out:

a) storage of input information;

b) inhibition of input information.

The schematic diagram of the module shown in Fig. 53 is analogous to the diagram of module FT-2 with respect to its principle of action and the number of elements entering it. Usually module FT-3 is used in conjunction with module FT-6.

Power drain at frequency f = 200 kHz is 2.1 W.

With respect to constructive shaping, size, and weight, module FT-3 is analogous to FT-2.

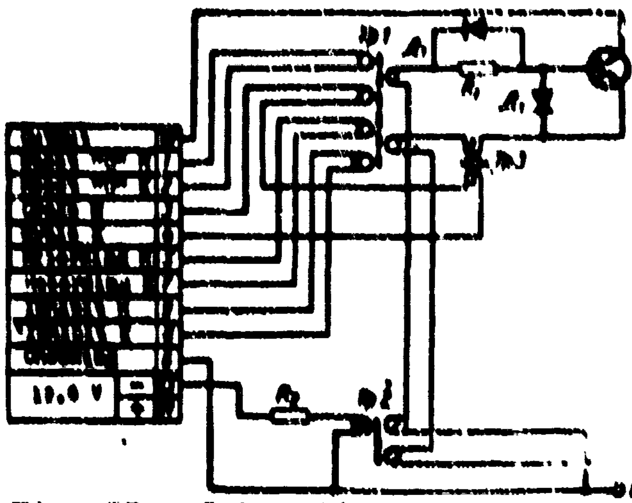


Fig. 53. Schematic diagram of FT-3.

Module FT-4

The module is a two-input coincidence circuit with a short delay time of output signals relative to input signals.

The coincidence circuit (Fig. 54) consists of two triodes T_1 and T_2 connected in series each of which is opened by a signal proceeding from the base windings of transformers Tr_1 and Tr_2, respectively, consisting of cores M2000-NM-1. Every triode is connected via the positive feedback circuit. Circuit R_3C_1 in conjunction with tranoformer Tr_1 determines the width of the output current pulse the amplitude of which is limited by resistor R_6.

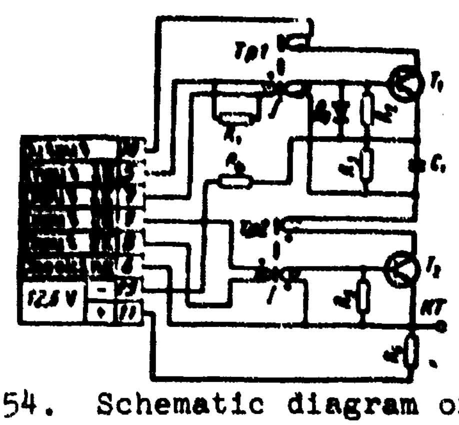


Fig. 54. Schematic diagram of FT-4.

The power consumed by the module at maximum frequency without load in the output circuit is equal to 0.4 W.

Structurally the module is analogous to module FT-1, and its size and weight are identical to those of FT-1.

Module FT-5

The FT-5 is an element delaying the input pulse the length of time equal to its width.

The schematic diagram of the module (Fig. 55) contains two transformers, Tr_1 and Tr_2, consisting of cores 0.25 VT (K-272) K2 × 1.4 × 0.8 and M2000-NM-1, respectively. The core of Tr_1 is in state 0 under the action of direct current flowing through the bias winding. Input information proceeding through the "Input" or "Cycle" winding shifts the core to state 1. Upon completion of this signal the core again returns to state 0.

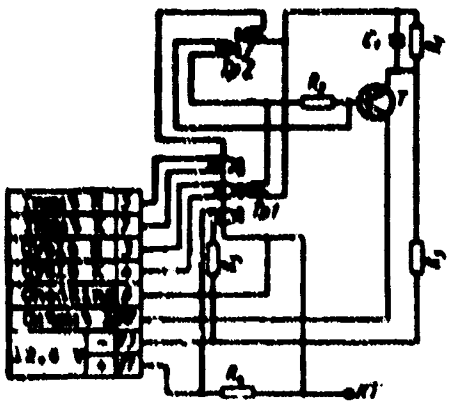


Fig. 55. The schematic diagram of module FT-5.

Triode T is unlocked. Transformer Tr_2 creates strong positive feedback between the collector and base current of triode T, saturating it. Divider R_3, R_1, R_4 creates reverse bias on the emitter of triode T.

Output pulse width is determined by circuit C_1, R_1 in conjunction with transformer Tr_1.

Constructive shaping is the same as that of modules FT-1 and FT-4.

Module FT-6

This module is the limiting resistor for modules FT-2 and FT-3. The schematic diagram of the module (Fig. 56) contains 6 24-Ω resistors divided into 2 groups. Every group forms an 8-Ω load.

The maximum permissible dissipated power for each load is 4 W.

The complex of modules FT was created as a standardized complex utilized in various devices of discrete automatics. At present the complex is permitted for wide use in new developments.

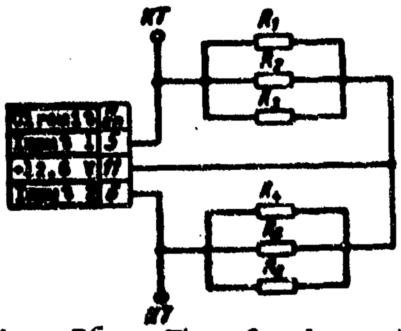


Fig. 56. The fundamental electrical circuit of module FT-6.

The electrical, load, and reliability characteristics of FT modules are given in Table 50.

The dimensions of the module are 34 × 24 × 19.

Table 53.

Designation of characteristic	Type of modules						
	А	Б	Г	Д	Е	Ж	И
Load capacity:							
active, in modules	5 modules А, Б, Г, Д, И or 2 modules Ж or 1 module Е	5 modules А, Б, Г, Д, И or 2 modules Ж or 1 module Е	5 modules А, Б, Г, Д, И	—	30 modules А, Б, Г or 15 modules Ж	3 modules А, Б, Г, И	Relay with 50 mA, operation current
Capacitive to ground in pF	75	100	300	—	500	100	—
Supply voltage in V	−30 −10 − 6,3 + 6,3	−30 − 6,3 + 6,3	−30 − 6,3 + 6,3	−30 — —	−30 − 6,3 + 6,3	−30 − 6,3 + 6,3	−30 −10 + 6,3
Consumed current in mA from source:							
−30 V	12	5,4	5,4	6	48	21	29
−10 V	12	—	—	—	—	—	40
−6,3 V	7,3	2,4	2,4	—	21	7,2	—
+6,3 V	2,9	0,85	0,85	—	12	0,85	1
Voltage on input in V:							
upper level	0—1,5	0—1,5	0—1,5	—	0—1,5	0—1,5	0—1,5
lower level	−6—7,9	−6—7,9	−6—7,9	—	−6—7,9	−6—7,9	−6—7,9
Voltage on output in V:							
upper level	−0,5—1,5	−0,5—1,5	−0,5—1,5	—	0,5—1,5	−0,5—1,5	—
lower level	−6—7,9	−6—7,9	−6—7,9	—	−6,6—9,5	−6—7,9	—
Number of logical possibilities on inputs of "AND" circuit	5	5	5	—	1	1	—
Number of logical possibilities on inputs of "OR" circuit	3	5	5	—	1	1	—
Dimensional in mm	55×34,8××22,3	54×34×12,5	54×34×12,5	54×34×5,5	54×35×22,5	55×34,8××22,3	54×34×12,5
Weight in g	27,5	15,7	15,7	11,8	33,5	38,8	17,3

Note: The number of logical possibilities of modules А, Б, and Г can be expanded on the inputs of the "AND" circuit to 300 and on the inputs of the "OR" circuit to 80.

2. Initial Setting Up of Logic Elements

Module A-1 (Fig. 62a) — a universal logic element — a two drift-transistor inverter. It carries out the "AND-NOT" function, and in conjunction with other elements various logic functions. Module A-1 with module Д-1 carries out the "AND-OR-NOT" function.

Module Б (Fig. 62b) is a universal logic element. It is a potential inverter consisting of a drift transistor with two-stage diode logic on input. The module carries out the function "AND" and "NOT" and in conjunction with other elements various logic functions. Module Б and module Д carry out the "AND-OR-NOT" function.

Module Г (Fig. 62c) is a universal logic element. It is an unsaturated potential inverter consisting of an alloy transistor with two-stage diode logic on output. It carries out "AND" and "NOT" and in conjunction with other elements various logic functions; in conjunction with module Д it carries out the "AND-OR-NOT" function.

Module Д (Fig. 62d) is two independent diode logic circuits realizing the functions "AND-OR" and "AND," depending upon the commutation of input and output terminals. It is intended for joint use with modules A, Б, and Г of the complex of elements of the Ural-10.

Module E (Fig. 62e) is the output stage of a power amplifier and is intended for amplification of signals in circuits of electronic computers and devices of discrete automatics. It switches up to 30 modules of type A, or Б, or Г.

Module Ж (Fig. 62f) is a kipp oscillator carrying out delay of positive voltage drop with a 5 μs delay width with an instability of ±10%. It is used as a delay element in electronic computers and devices of discrete automatics.

Module И (Fig. 62g) is an inverter intended for work on a relay with a consumed current of not more than 50 mA and a voltage of 10 V and for realization of light indication.

3. Recommendations for Application of the Modules of the Ural-10 Complex

For a developer using a complex of model elements of modules it is important to know not only their basic electrical and reliability characteristics, but also the basic conditions of their application.

The basic conditions of application of modules of the Ural-10 complex boil down to the following firm recommendations.

All elements of the Ural-10 complex will agree with each other with respect to input and output.

In recommendations on the modules of the Ural-10 complex there are shown the most wide-spread cases of connection of modules; however, there can also be other connections not shown in the recommendations; there is not allowed disturbance of conditions of coordination of levels and thermal and electrical conditions of completing articles.

In the recommendations there are stipulated the conditions of work of various types of modules with a cable having wave impedance of 50, 75, and 150 Ω, and also with model delay lines with wave impedance of 600 and 1200 Ω.

In the "Recommendations" there are given examples of the application of modules in logic circuits. These solutions are not single during construction of electronic computer subassemblies and devices of automatics consisting of standardized Ural-10 modules.

The use of the Ural-10 modules in accordance with the present recommendations ensures the reliable work of the modules under the most difficult conditions in the temperature range -10 to +50°C.

In the appendix to the present recommendations there is given the character of change of switching with expansion of logic possibilities and with change of load capacity with respect to the first and fourth contact output. In the same place there are given graphs of distribution of switching times and dependence on temperature in the range -60 to +70°C.

a) General requirements

The modules of a Ural-10 complex of type А-1, Б-1, Б-2, Г-1, Г-2, Д-1, Е-1, Ж-1, and И-1 must be exploited under the conditions stipulated by the general technical conditions for standardized circuit elements (modules) of electronic computers and devices of discrete automatics, i.e., under conditions:

a) lowered temperature to -10°C;

b) raised temperature to +50°C;

c) relative humidity of 98% at a temperature of +32°C;

d) vibrations of frequency 20-80 kHz with accelerations of 4-10 g;

e) impact loads with acceleration to 35 g.

Stability of feed voltages should be not worse than ±10% of the nominal values shown in the drawings.

Standard signals of the modules of the Ural-10 complex in the whole temperature range are signals with upper level u_B = -0.5 to +1.5 V and lower u_H = -6 to -7.9 V.

According to firm indications there is allowed work of the modules of the Ural-10 complex from signals with nonstandard voltage levels:

$$-1.5\ \text{V} < u_в < 0\ \text{V};$$
$$-10\ \text{V} < u_н < -6\ \text{V}.$$

If the lower voltage level of the signal at the input of the "AND" circuit of modules of type А-1, Б-1, Б-2, Г-1, and Г-2 is nonstandard, then the second input of the "AND" circuit should be fed a signal with standard levels or voltage -6.3 V ±10%.

All types of modules have to be used in model connection according to Table 54 and in accordance with the given recommendations.

Table 54.

No. in order	Type	From which modules it can work: Type of modules	Leads: Output	The given module — Leads: Input	The given module — Leads: Output	To which modules it can work — Leads: Input	To which modules it can work: Type of modules	The maximum number of "AND" circuit inputs for each "OR" circuit input	Maximum number of "OR" circuits	Permissible load — Number of modules: А, Б, Г, Д, И	Permissible load — Number of modules: Е	Permissible load — Number of modules: Ж	Permissible load capacity in pF with respect to "ground": To lead "1"	Permissible load capacity in pF with respect to "ground": To lead "2"	Permissible load capacity in pF with respect to "ground": To lead "3"	Note
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
1	А-1	А, Б, Г Е, Ж Д	13 1 (13) 2, 3, 4 (10, 11, 12)	2, 3 9, 10, 11 4	13	2,3 2 3,4 (10, 11, 12)	А, Б, Г Е, Ж, И Д	5	—	5	1	3	—	5	75	With increase in the number of "OR" circuits time parameters are not guaranteed
2	Б-1	А, В, Г Ж, Е Д	13 1 (13) 2, 3, 4 (10, 11, 12)	2,3 1 4	13	3,3 2 2, 3, 4 (10, 11, 12)	А, В, Г Е, Ж, И Д	5	5	5	1	3	30	20	100	
3	В-2	А, В, Г Е, Ж Д	13 1 (13) 2, 3, 4 (10, 11, 12)	2,3 1 4	13	2,3 2 2, 3, 4 (10, 11, 12)	А, Б, Г И, Ж Д	5	5	3	—	1	30	20	100	
4	Г-1	А, В, Г Е, Ж Д	13 1 (13) 2, 3, 4 (10, 11, 12)	2,3 1 4	13	2,3 2 2, 5, 4 (10, 11, 12)	А, Б, Г И, Ж Д	5	5	5	—	—	100	75	300	
5	Г-2	А, В, Г Е, Ж Д	13 1 (13) 2, 3, 4 (10, 11, 12)	2,3 1 4	13	2,3 2 2, 3, 4 (10, 11, 12)	А, В, Г И, Ж Д	5	5	3	—	—	100	75	300	
6	Д-1	А, В, Г Ж, Е	13	2, 3, 4 (10, 11, 12)	1 (13) 2, 3, 4 (10, 11, 12)	1 (13) 10, 11 4	Д А, В, Г, И	—	—	—	—	—	—	—	—	Capacitance is stipulated for leads of modules to which module to which module Д is connected

Table 53. (Cont'd).

No. in order	Type	From which modules it can work		The given module		To which modules it can work		The maximum number of "AND" circuit inputs for each "OR" circuit input	Maximum number of "OR" circuits	Permissible load			Permissible load capacity in pF with respect to "ground"			Note
		Type of modules	Leads				Type of modules			Number of modules						
			Output	Input	Output	Input				[illegible]	Е	Ж	To lead "1"	To lead "2"	To lead "13"	
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
7	Е-1	А, В, Г Е	13	2	13	2,3 2 2, 3, 4 (10, 11, 12)	А, В, Г Е, И, Ж Д	—	—	30	1	15	—	—	500	
8	Ж-1	А, В, Г Е, Ж	13	2,3	13	2,3 2 2, 3, 4 (10, 11, 12)	А, В, Г И, Ж Д	—	—	3	—	1	—	—	100	Input Output
9	И-1	А, В, Г Е, Ж Д	13 1 (13)	2 1	12 13	—	Tube of type МБМ, relay	—	—	—	—	—	—	—	—	The current of operation of the relay is not more than 50 mA

Note: 1. Leads shown in graphs 11, 12, and 13 are mutually exclusive.

2. If in the table there is not indicated modification of the module – there is no index (for example Б, Г) – then the requirements are extended to all modifications of the given groups (Б-1, Б-2, Г-1, Г-2).

3. With increase in capacity leads stipulated in graphs 14, 15, and 16, the time responses of the modules are not guaranteed.

4. The numbers in parentheses signify the number of the lead.

There is allowed unification of outputs of modules of one type A-1, Б-1, Б-2, Г-1, Г-2, and Е-1; the load capacity will be:

for modules Б-1, Б-2, Г-1, and Г-2

$$N = N_0 - (m - 1);$$

for module A-1

$$N = N_0 - 3(m - 1);$$

for module E-1

$$N = N_0 - 10(m - 1).$$

where N_0 is the load capacity (coefficient of branching) of the module; m is the number of integrated modules.

For example, with the integration of the outputs of three modules of type Б-1 we have

$$N_0 = 5, \quad m = 3;$$
$$N = 5 - (3 - 1) = 3.$$

<u>Note</u>: If there are no crosspieces between leads 12 and 13 of the integrated E-1, then the load capacity N will be $N = N_0$, but the number of united modules should not be more than ten.

The logical possibilities of modules of type A-1, Б-1, and Г-1 can be expanded (with impairment of time properties) according to the following formulas:

$$M < \frac{300}{q} \text{ when } K < 5 \text{ and } N_0 < 5; \tag{5}$$

$$K \leqslant 108 - 20{,}6N_0 \text{ when } M < 5, \tag{6}$$

where q is the load (coefficient of branching of the preceding module); K is the number inputs of the "OR" circuit of the examined module; M is the number of inputs of the "AND" circuit of the examined module; N_0 is the load (coefficient of branching) of the examined module.

Figure 63 gives an example of expansion of the logic possibilities of module Б-1.

Let us determine whether it is possible to expand the logic possibilities of module Б-$1_{(2)}$ to $M_{(2)} = 20$, when $K_{(2)} = 5$, $N_{0(2)} = 3$, $q = 3$.

By formula (5) we find that the number of "AND" circuit outputs of module Б-$1_{(2)}$ can be

$$M < \frac{300}{q} = \frac{300}{3} = 100.$$

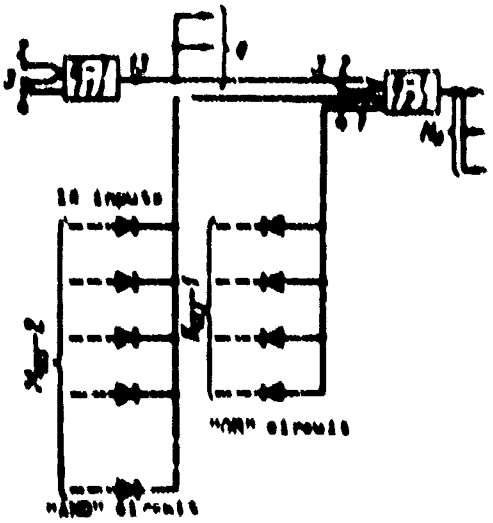


Fig. 63. An example of the logic possibilities of the module.

In our case $M_m = 20 < 100$.

__Note:__ Work of the module with expanded logic directly to the memory element (for example, register) without additional planning is not allowed.

Leads 1 and 4 of modules Б-1, Б-2, or Г-1, Г-2, and leads 1, 10, and 11 of module A serve to connect module Д or the same diode circuits of another design.

The number of "AND" circuit inputs can be attained by connection to lead 1 of single diodes by suspended wiring.

Average delay time measured at a level of 0.5 drop in a long chain of n elements of the same type in the temperature range -10 to $+50^{\circ}$C can be defined as $\bar{\tau}_3 = n t_3$, where $\bar{\tau}_3$ is the average delay time introduced by one module in a long chain of modules of one kind.

The average delay time $\bar{\tau}_3$ of one module in the temperature range -10 to $+50^{\circ}$C is given in Table 55. The idea of average delay time $\bar{\tau}_3$ is valid when $n > 3$. When $n \leq 3$ the delay time for the module should be considered equal to the switching time, which is stipulated in the corresponding particular technical conditions for the given type of module.

__Note:__ The value of $\bar{\tau}_3$ is definitized after accumulation of experimental material.

Table 55.

Parameter	Type of module		
	A	Б-1, Б-	Г-1, Г-2
T_0 in μs	0,07	0,2	1,2

To protect the transi tors of every cell or block from excess of maximum permissible voltage on the collector of the closed triode due to the disappearance of fixing voltage ($E_\Phi = -6.3$ V) the voltage source E_Φ in the cell or block should be shunted by resistance. Shunting resistance $R_\text{Щ}$ is selected in such a manner that voltage drop at it in the absence of voltage E_Φ at the expense of the load currents of the given cell or block does not exceed the least of the maximum permissible voltages at the collector for the transistor used.

The shunting resistance for a cell or block of modules of one type can be determined from the inequality

$$R_\text{ш} < \frac{E_{\Phi\,\min} R_\text{к}}{(E_{\text{к}\,\max} - E_{\Phi\,\min})n}, \tag{7}$$

where $R_\text{К}$ is the collector resistance of the modules in the cell or block; n is the number of modules in the cell or block, $E_{\Phi\ \min}$ is the fixation voltage $-$ 10% of the value of $E_{\Phi\ \text{НОМ}}$; $E_{\text{К}\ \max}$ is the voltage of the collector source +10% of the value of $E_{\text{К}\ \text{НОМ}}$.

If the cells of blocks are composed of modules of various types, then the latter inequality takes on the form

$$R_\text{ш} < \frac{E_{\Phi\,\min} R_\text{э}}{E_{\text{к}\,\max} - E_{\Phi\,\min}}. \tag{8}$$

where $R_\text{Э}$ is the total value of the collector resistances of the modules in the cell or block.

The total shunting resistance of all the cells or blocks which load the fixation source should satisfy the inequality

$$R'_\text{ш} \geqslant \frac{E_{\Phi\,\max}}{I_{\text{н}\,\max}}, \tag{9}$$

where $E_{\Phi\ max}$ is the maximum voltage of the fixation source; $I_{\Pi\ max}$ is the maximum current-carrying capacity of the source of fixation voltage E_{Φ} = -6.3 V.

The switching on and operation of the modules in the absence of 6.3 V bias voltage are impermissible.

In designing cells and blocks it is necessary to provide for measures excluding accidental closing of leads carrying feed voltage with the leads of inputs or outputs of modules. It is recommended, for example to have a grounded lead between leads carrying supply voltage and leads of inputs and outputs of modules.

Thd modules can work to delay lines of types [LZ] (Л3) [LZT] (Л3Т). The input of the delay line can be any LZ lead. The output from the delay line can be only from the end of the delay line.

During the work of the modules on the delay line (Fig. 64) the output of the latter should be coordinated with help of external resistance R_1 (value – see Table 55), connected to the 6.3 V source of fixation voltage.

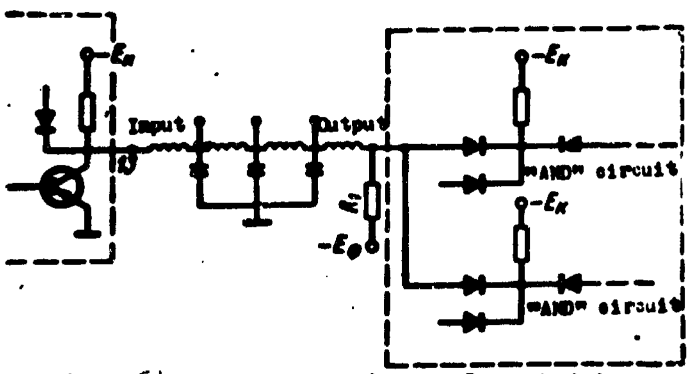


Fig. 64. Connection of matching impedence R_1 to the output of the delay line during the work of the module to the full delay line.

At the input of the delay line with ρ = 1200 Ω there can be the modules A-1, Б-1, Б-2, and Е-1, and at the output of the delay line with ρ = 600 Ω the modules A-1, Б-1, and E-1.

Note: With a load of the output of the delay line of more than one module, gating of the "AND" circuits connected to this output is not allowed.

During the work of the modules to part of the delay line (Fig. 65) both ends of the delay line should be coordinated by external resistances R_1 and R_2, connected to source of fixation $E_\Phi = -6.3$ V (the values of the resistances are given in Tagle 56). At the input of the delay line with wave impedance $\rho = 1200\ \Omega$ there can be modules of type A-1, Б-1, E-1, and at the input of the delay line with $\rho = 600\ \Omega$ only a module of type E-1.

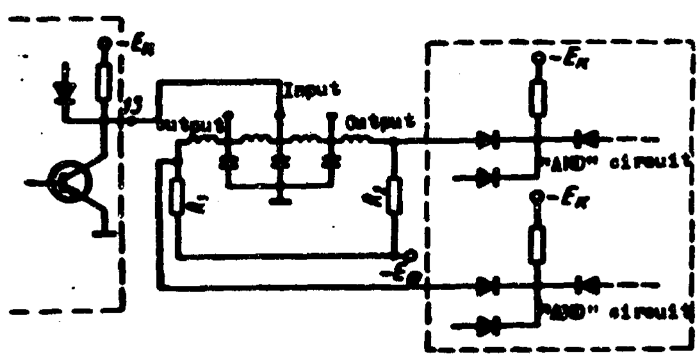


Fig. 65. Connection of matching impedances R_1 and R_2 to the outputs of the delay line during the work of the module to part of the delay line.

Table 56. Coordination of delay-line outputs.

ρ	Number of modules А, Б, Г	Tentative values of matching impedances in Ω	ρ	Number of modules А, Б, Г	Tentative values of matching impedances in Ω
600	0 1 2	620 820 1100	1200	0 1 2	1200 2000 4300

The average delay time $\bar{t}_3$ of one module in the temperature range from -10 to +50°C.

Work to radio frequency or pulse cable can be carried out only from a module of type E-1 via the circuit shown in Fig. 66. Leads 12 and 13 of module E-1 have to be opened.

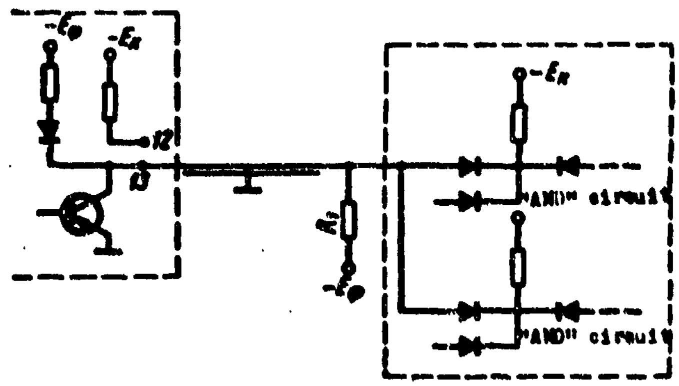


Fig. 65. Connection of matching impedence R_1 during the work of a module of type E to a radio frequency or pulse cable.

The conditions of coordination of the cable with wave impedances of 50, 75, and 150 Ω are given in Tables 57, 58, and 59, respectively.

Table 57. Wave impedance of cable ρ = 50 Ω.

Number of types of "AND" circuits at cable output	1 or 2	From 3 to 5	20
Tentative value of matching impedance in Ω.................	56	62	91

Table 58. Wave impedance of cable ρ = 75 Ω.

Number of model "AND" circuits at output of cable	1 or 2	From 3 to 5	20
Tentative value of matching impedance in Ω.................	82	91	180

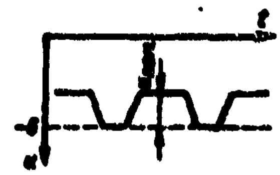
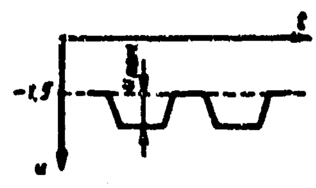
Table 59. Wave impedance of cable ρ = 150 Ω.

Number of model "AND" circuits at output of cable	1 or 2	From 3 to 5	20
Tentative value of matching impedance in Ω.................	160	180	910

Switching on of modules with extreme parameters at the input and output of the cable or delay lines is not allowed.

The value of potential interference at the input of the modules at a temperature of +20°C should not exceed the values given in Table 60.

Table 60.

Type of module	А-1, Б-1	Б-2, Г-1, Г-2	Oscillogram at input of module
Permissible amplitude of interference at -6.0 V level	+1,0	+0,6	
Permissible amplitude of interference at 1,5 V level	−0,5	−0,5	

b) <u>Peculiarities of application of elements of the Ural-10 complex</u>

<u>Module A-1</u>. Leads 10 and 11 of A-1 modules serve to connect only module Д-1. Leads 10 and 11 are inhibited from being connected to lead 13 of all modules besides module Д-1.

To form an "OR" circuit it is necessary to connect lead 10 or 11 of module A-1 to lead 1 or 13 or module Д-1. Leads 5 or 9 of module Д-1 must be connected to the -30 V voltage source.

To form an "OR" circuit it is permissible to use lead 4 of module A-1; the switching time of the module can differ from the time indicated in the [TU] (TY) [technical specification] norms.

<u>Module Д-1</u>. All the points listed below are valid for each half of Д-1.

To form an "OR" circuit module Д-1 is connected by lead 4 (lead 2 or 3) to lead 4 of one of the modules Б-1 or Г-1, and lead 5 is fed -30 V.

The inputs are the vacant outputs of leads 2, 3, and 4.

To form an "OR" circuit module Д-1 is connected by lead 1 to lead 1 of one Д-1 module, which will form "OR," as shown above. Voltage is not supplied to lead 5. The inputs are leads 2, 3, and 4.

The values of matching impedances during work of a module of E-1 on the cable are represented in Tables 57, 58, and 59.

The value of potential interference at the input of the module at a temperature of +20°C is shown in Table 60.

To form an "OR" circuit at the input of module A-1 module Д-1 is connected by lead 1 to lead 10 or 11 of only one A-1 module. Lead 5 of module Д-1 is fed -30 V. The inputs will be leads 2, 3, and 4.

To form an "AND" circuit module Д-1 is connected by lead 1 to lead 1 of one of the modules A, Б, and Г. Lead 5 of module Д-1 is not fed voltage. The inputs are leads 2, 3, and 4.

The input of module Д-1 is equivalent in load to standard input A, Б, Г, and И.

<u>Module E-1</u>. The module has a nonstandard lower level of voltage; therefore, one of the outputs of the "AND" circuit of any module working from module E-1 should be fed a signal with standard levels of voltage, or the free input should be fed -6.3 V fixation voltage. The levels of output signals for modules A-1 or B-1, working to module E-1, are nonstandard.

Module E-1 should be located in immediate proximity to module A-1 or Б-1 with a length of connecting wires of not more than 10 cm.

Lead 13 of modules A-1 or Б-1, working to module E-1, is not allowed to be connected to other modules.

During work of module E-1 to nonstandard loads it is necessary that the current through the fixation diode not exceed 30 mA.

During the work of module E-1 lead 12 must usually be closed with lead 13. During the work of module E, leads 12 and 13 are not closed to the cable. The matching impedance is connected at the end of the cable in accordance with point 18 of the present recommendations.

Module И-1. During the work of module И-1 lead 10 should be grounded to an incandescent tube of type [NSM] (HCM). A -10 V source is connected through tube NSM to lead 12. To increase the brightness of glow of the lamp the use of a -12.6 V source instead of a 10 V source is permitted.

During the work of module И-1 on a relay with a current of operation of not more than 50 mA, a supply voltage of -10 V (or 12 V) is fed through the relay winding to lead 13. The grounding of lead 10 is not allowed. The relay winding must be shunted by a diode (plus to source).

In low-frequency circuits module И-1 can be used as a powerful amplifier with a load capacity of 15 modules Б, Г, and a switching time of about 15 μs.

To switch on module И-1 as a power amplifier it is necessary to connect lead 16 of module И-1 with lead 1 or 13 of module Д-1, and feed one of the leads 2, 3, 4, or 10, 11, 12 of module Д-1 -6.3 V fixation voltage, and to feed lead 9 or 5 of module Д-1 -30 V. Similarly instead of module Д-1 it is possible to use one of the inputs of modules Б, and Г.

The output of the power amplifier is lead 13 of module И-1.

In conjunction with module Д-1 the И module can carry out logic operation "AND-NOT."

The basic logic possibilities of the Ural-10 complex. The Ural-10 complex was developed taking into account the possibility of construction directly on its elements of basic logic circuits of electronic computers and device of discrete automatics.

Modules of the Ural-10 type can be used in the following circuits:

a) A register for storage of one binary digit (P_r).

b) A one-bit counter for recalculation of sequence of signals ([Sch] (Cч)).

c) A shifter.

d) A one-bit three-input adder.

e) A one-bit five-input adder.

f) A decoder.

g) A controlled generator of a series of pulses.

h) A pulse shaper.

The register shown in Fig. 67 is two amplifiers interconnected by positive feedbacks. Such a circuit has two stable states.

As amplifiers there can be used modules A, Б, or Г.

Inputs 2 of the modules are used to form feedbacks.

Inputs 3 can be used to record 0 or 1 in the register (reset the register to 0 and 1) by positive pulses (u_B). The register Pr can be switched by negative signal u_H, fed to input 4 of the module through module Д. Switching is carried out when a signal is supplied to a locked triode.

The duration of the starting signal should be not less than (1.5 + 2.0) $t_{\text{пер}}$.

The load capacity each register output is

$$N_{Pr} = N_0 - 1,$$

where N_0 is the load capacity of one module; $t_{\text{пер}}$ is the switching time of a given type of module.

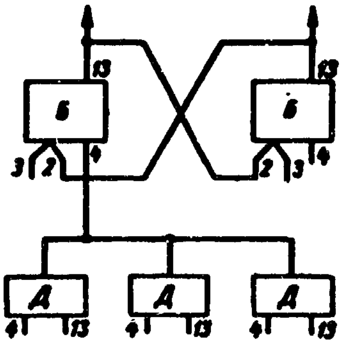


Fig. 67. Functional diagram of register.

The potential one-bit counter is shown in Fig. 68. It consists of two registers, where the second duplicates the state of the first and also switches the input signal proceeding to the "counter" input to the one or zero input of the first register.

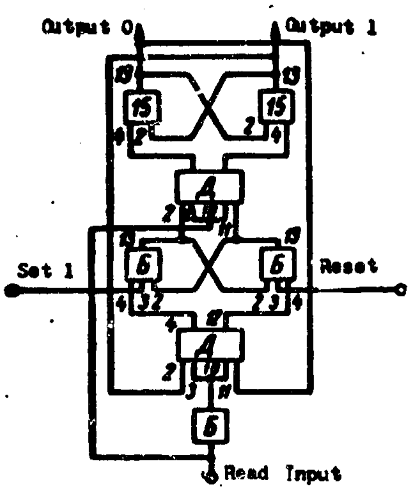


Fig. 68. The functional diagram of the potential counter.

The change of state of the second occurs only after the termination of the input signal. From a one-bit counter there can be formed a chain of counters for recalculation of the sequence of pulses.

A reversible shifter is shown in Fig. 69. It consists of two registers. The shift is carried out in the auxiliary register by the

rewriting of the contents of the n bit in the n + 1 bit (shift to the right) or in the n - 1 bit (shift to the left). On the following pulse the shifted number is rewritten in the main register.

The circuit of a one-bit adder of code-position three-input type (Fig. 70) is for addition of values A and B and for transfer from the low-order bit to the high-order bit. The circuit realizes the logic function in accordance with the following equations:

$$\left.\begin{aligned}
c &= \overline{\left[p\,\overline{(AB + AB)} + p\,\overline{(A\bar{B} + \bar{A}B)}\right]};\\
\bar{c} &= \overline{\left[p\,\overline{(A\bar{B} + \bar{A}\bar{B})} + \bar{p}\,\overline{(AB + \bar{A}\bar{B})}\right]};\\
Q &= \overline{\left[\bar{A}\bar{B} + \overline{(AB + \bar{A}\bar{B})}\,\bar{p}\right]};\\
\bar{Q} &= \overline{\left[AB + \overline{(AB + \bar{A}\bar{B})}\,p\right]}.
\end{aligned}\right\} \qquad (10)$$

Here c is the sum; Q is the transfer to the high-order bit.

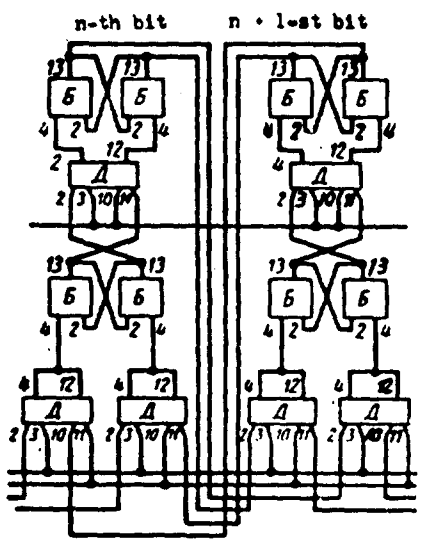


Fig. 69. The functional diagram of the reverse shifter.

The decoder depicted in Fig. 71 is a series of single-stage coincidence circuits on low input levels of signals.

The controlled pulse series generator is depicted in Fig. 72. It can consist of modules A or Б and delay lines of type LZ or LZT. The generator puts out a series of pulses in the presence of a permitting

signal at the control input (lead 2). Tentatively the pulse repetition rate can be determined by the formula

$$f = \frac{1}{2} \cdot \frac{1}{\tau_{зад}},$$

where $\tau_{зад}$ is the duration of LZ delay.

The pulse shaper shown in Fig. 73 can consist of two modules of one type A or B and a delay line of type LZ or LZT.

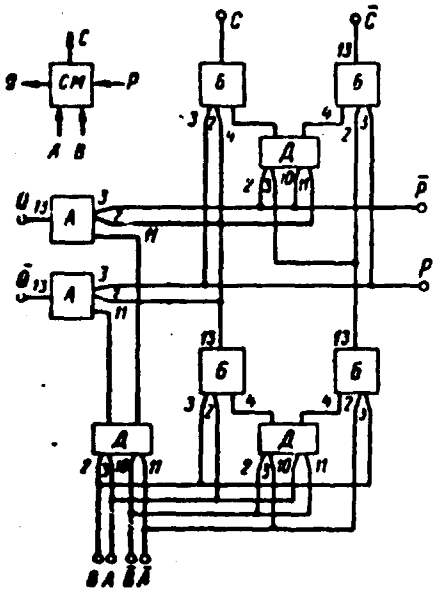


Fig. 70. Three-input adder.

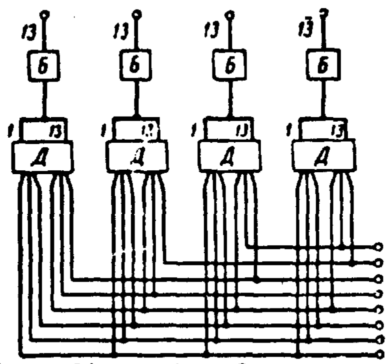


Fig. 71. The functional diagram of the decoder.

Upon the entering of input 2 by a pulse or drop of negative polarity of standard amplitude at leads 13 there are obtained pulses

of different polarity equal to $t_{зад}$ in width.

With increase in load capacity at leads 1 or 13 higher than the permissible load stipulated in Table 54, through the triode there can flow a pulse current $I_{K\ имп}$ considerably exceeding static current $I_{ст}$. Therefore, it is necessary to measure collection current I_K according to the diagram of Fig. 74 and to make sure that the collector current in the pulse is less than the maximum permissible current shown in the TU for the given triode.

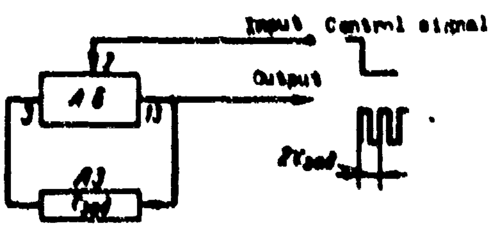


Fig. 72. Controlled series generator.

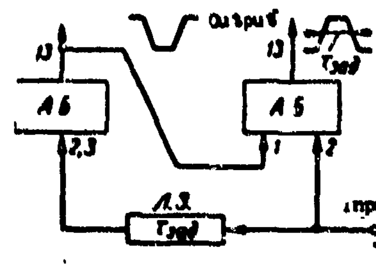


Fig. 73. Pulse shaper.

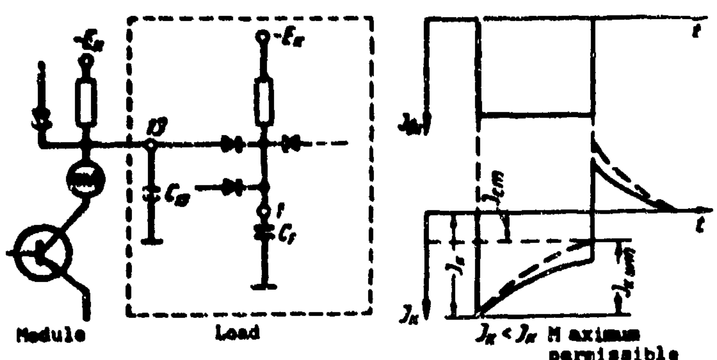


Fig. 74. Circuit measuring collector current with load capacity increase at leads 1 or 13 higher than what is permissible.

5.8. Recommendations for the Application of a Model Complex of Elements at a Frequency of 250 kHz[1]

With the cells of a complex of standardized functional circuit elements at a working frequency of 250 kHz it is possible to construct general-purpose and special-purpose computers and also individual units of a system of discrete automatics.

For the normal functioning of every cell in the designed unit it is necessary to observe the following basic rules:

1. The cells with respect to the influence of climatic and mechanical factors satisfy the requirements of the interindustrial standard.

2. There is not allowed the switching on of cells under tension without checking the absence of short circuits between grounds and feed buses and between feed circuits and cell output.

3. When a cell is checked, the face value of each feed voltage is allowed to vary ±10%.

4. The parameters of the input signals and the value of loads of one type have to lie within the limits prescribed in the TU.

5. The value of the maximum permissible capacitive loads (C) and static input (I_{BX}) and output ($I_{BЫX}$)currents for every type of cell must not exceed the values shown in Table 61 and must satisfy the following relationships:

$$C \geqslant C_{мон} + \Pi_1 C_{вх}; \tag{11}$$

$$I_{вх} \geqslant \Pi_2 i_{вх} + \Pi_3 i_{вых}; \tag{12}$$

$$I_{вых} \geqslant \Pi_4 i_{вых} + \Pi_5 i_{вых}. \tag{13}$$

where C_{MOH} is the total capacity of the assembly wires the equivalent values of which are given in Table 62; C_{BX} is the input capacity of the cells given in Table 63; i_{BX}, $i_{BЫX}$ are the static input and output currents for the various types of inputs given in Table 63; Π_1-Π_5 is the number of loads.

Table 61.

Cell parameters	Type of cell						
	1Ф1, 1Ф2	1Ф3	И	1Д1	1Д2	1П	1Тг
Input current in mA.......	7	90	7	7	7	30	7
Output current in mA......	—	—	4	4	4	40	4
Load capacity in pF.......	200	1000	1000	100	100	4000	1000

Table 62. Capacity between conductors with length of conductors l = 1 m.

Kind of wiring	Distance between conductors			
	1 мм	2 мм	5 мм	10 мм
Wire with a diameter of 0.1 mm....	—	18	14	12
Wire with a diameter of 0.5 mm....	—	40	24	18
Wire with a diameter of 1 mm......	2	80	35	24
Printed circuit..................	80	—	—	—

Table 63.

Cell parameters	Type of input						
	Pulse-potential valve		1М	1Д$_1$	1Д$_2$	1П	1Тг
	Connection to potential element	Connection to pulse element					
Input current in mA...	0,15	—	—	1,6	1	1,5	—
Output current in mA..	—	1,6	2	—	—	6	—
Input capacity in pF..................	10	10	100	30	15	170	200

The permissible number of various types of loads for every cell is determined from conditions (10), (11), and (12).

6. One input of each unutilized valve in cells 1Ф$_1$, 1Ф$_2$, and 1Ф$_3$ should be grounded.

7. The output of the delay lines in cell 1т can be connected to the inputs of any types of shapers, where the length of the connecting wire should be not more than 1 m. There is not allowed simultaneous use of more than one output of the delay lines.

8. When there must be a greater number of valves than there are in one shaper, it is possible to unite up to four shapers of type 1Ф$_1$ on output.

Note: In the absence of parallel connection of shapers 1Ф$_1$ output pinches 23 and 24 are connected by external wiring.

9. Computing input and the setting of the trigger to 0 and 1 are carried out with the help of gating at the inputs of shapers.

10. To avoid variation in standard levels no more than two 1Д$_1$, 1Д$_2$, and 1П cells are allowed to be connected in series.

11. For visual observation of the state of the flip-flop it is necessary to connect the indicated output of cell [1Tg] (1Tr) with the input of the circuit shown in Fig. 75.

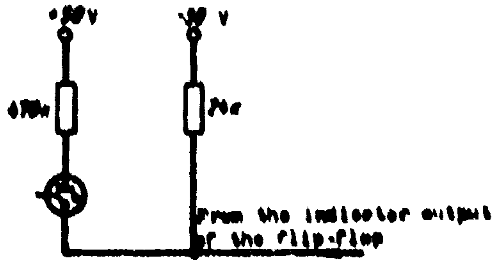


Fig. 75. Connection of cell Tg with the output of the circuit for visual observation of the state of the trigger.

12. The output of cells 1Ф$_1$ and 1Ф$_2$ can be simultaneously loaded only on one output of the delay line and on one input of the pulse-potential valve.

13. The shapers in cells 1Ф$_1$ and 1Ф$_2$ can operate in two modes: amplification on leading edge of input pulse; amplification on trailing edge of input pulse.

<u>Note</u>: a) the shapers in cells 1Ф$_1$ and 1Ф$_2$ operate in the second mode only when they are connected to the flip-flop input.

b) in cell 1Ф$_1$ external wiring connects pinches 9 with 10 and 11 with 12 during operation in the first mode and 9 with 11 and 10 with 12 during operation in the second mode.

c) in cell 1Ф$_2$ external wiring connects pinches 9 with 10, 11 with 12, 16 with 20, and 21 with 22 during operation in the first mode and 9 with 11, 10 with 12, 16 with 21, and 20 with 22 during operation in the second mode.

5.9. A Complex of 20, 150, and 350 kHz Model Potential Elements

The complex of the system of potential elements ([SPE] (СПЭ)) [GSKTB] (ГСКТБ) [Translator's Note: expansion of acronym unknown] consists of three logic and seven auxiliary elements, during the use of which it is possible to collect any devices of computer technology and discrete automatics.

The complex of logic elements of the SPE contains three logic modules: [ML1] (МЛ1), ML2, and ML3.

Auxiliary elements ([VE] (ВЭ)) fulfill nonlogic functions in logic circuits (amplification, light indication, formation of pulses). The complex of auxiliary elements consists of the following units:

- the time-assigning stage [KVz] (КВз);

- the register element [ERg] (ЭРг);

- emitter repeater [PEm5] (ПЭм5);

- emitter repeater PEm6;

- indication elements [EI1] (ЭИ1) and EI2;

- the diode assembly [SD] (СД).

The elements the system are made out of plates with printed circuit in volume performance.

The maximum frequency of work of elements under various conditions is represented in Table 64, and the applicability of elements in certain frequency and temperature ranges is represented in Table 65.

The logic elements are intended for various frequency ranges:

logic module ML1 at a frequency of up to 20 kHz;

logic module ML2 at a frequency of up to 150 kHz;

logic module ML3 at a frequency of up to 350 kHz.

The principle of action of the basic logic and auxiliary elements of the [KPE] (КПЭ) complex is briefly described below.

Table 64.

Conditions			Frequency of elements in kHz				
t в °C	$E_к$ в в	$E_б$ в в	МЛ1	МЛ2	МЛ3	ПЭм5	ПЭм6
+70	−6,93	+5,67	—	196	—	712	250
+70	−6,50	+6,10	—	200	—	712	278
+50	−6,93	+5,67	26	240	333	555	350
+20	−6,93	+5,67	33	312	414	712	510
+20	−6,30	+6,30	34	345	473	485	526
+20	−5,67	+6,93	63	370	555	328	500
−10	−5,67	+6,93	80	462	660	303	205
−60	−5,67	+6,93	—	550	—	[illegible]	240
−60	−6,10	+6,50	—	588	—	225	240

Table 65. Application of elements in various frequency and temperature ranges.

Maximum frequency	Range of temperatures	
	from −10 to +50°C or from +5 to +50°C	from −50 to +70°C
20 kHz	КПЭ-20-НХ: МЛ1, КВз, ПЭм5, ПЭм6, ЭИ1, ЭРг, СД	—
150—200 kHz	КПЭ-200-НХ: МЛ2, КВз, ПЭм5, ПЭм6, ЭИ1, ЭРг, СД	КПЭ-150-СП: МЛ2, КВз, ПЭм5, ПЭм6, СД, ЭИ2, ЭРг
[illegible]0 kHz	КПЭ-350-НХ: МЛ3, КВз, ПЭм5, ПЭм6, ЭИ1, ЭРг, СД	—

Note: KPE – complex of potential elements; [Nh](НХ) – national economy; [SP] (СП)

1. Logic Elements

Logic module ML1. The module is a phase-reversing amplifier with three independent inputs working in relay conditions and realizing universal switching function "NOT-OR" (negation of disjunction or "Pierce arrow"), and ensures construction of any logic circuits, no matter how complicated.

Depending upon potentials at inputs element ML1 can be in two states: one or zero. The active element of the module – the triode is either in a state of cutoff (locked triode) or in a state of saturation (open triode), respectively.

The electrical schematic diagram of ML1 is represented in Fig. 76.

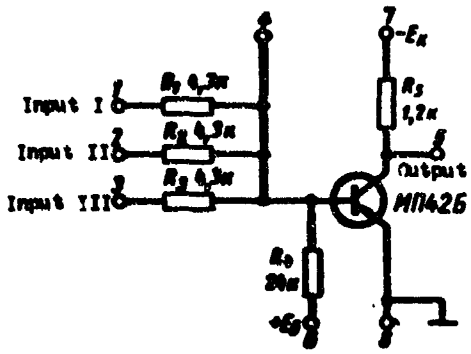


Fig. 76. The electrical schematic diagram of logic module ML1.

ML1 preserves its efficiency and ensures the stability of electrical characteristics under the following conditions:

change of ambient temperature from +5 to +50°C;

voltage of bias sources +5.3 ± 0.63 V;

voltage of power supplies -6.3 ± 0.63 V;

operating frequency up to 20 kHz;

resistive load of not less than 1000 Ω;

capacitive load of not more than 160 pF;

Input impedance of ML1 of 4500 Ω.

Source of positive voltage E_σ ensures reliable closing of the triode in the whole ambient-temperature range if at not one of the inputs there is a potential different from zero. The potential, not

differing from zero (for ML1) should be considered a voltage not lower than 0.2 V. The basic characteristics of ML1 are represented in Table 70.

The dimensions of the module are 26 × 21 × 14 mm.

Logic module ML2. With respect to the number of inputs, transfer characteristic, and logic properties, the module is completely similar to module ML1.

Logic module ML2 differs from ML1 only by the triode used in it [P416B] (П416Б) and its high resistance $R_б$ = 30 kΩ.

The electrical schematic diagram is shown in Fig. 77.

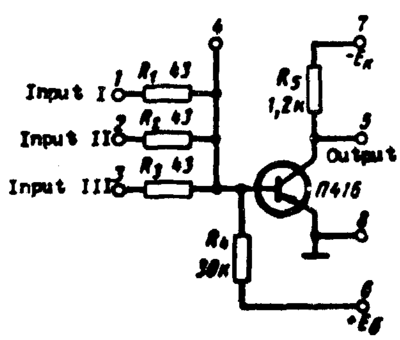


Fig. 77. The electrical schematic diagram of logic module ML2.

In the presence of at least one input of potential lower than the value corresponding to the one level, the triode is in saturation.

To keep the transistor from going out of order it is recommended that the power supplies be connected in a certain order: in the beginning power supply $E_к$, and then bias source $E_б$.

During the use in ML2 of only one input, it is desirable to ground any of the free inputs.

ML2 preserves efficiency and ensures the stability of electrical characteristics under the following conditions:

change of ambient temperature from -60 to +70°C;

power supply voltage of -6.3 ± 0.63 V;

bias source voltage of +6.3 ± 0.63 V;

operating frequency of up to 150 kHz;

resistive load of not less than 1500 Ω;

capacitive load of 50 pF.

The ML2 can be used in the range of temperatures from -10 to +50°C, maximum frequency should be not higher than 240 kHz, and the resistive load is not less than 1000 Ω.

The input impedance of ML2 is not less than 4500 Ω.

The dimensions of the module are 26 × 21 × 14 mm.

<u>Logic module ML3</u>. The electrical schematical diagram is shown in Fig. 78. To increase the speed of the module in the circuit there is used nonlinear feedback (diode [D9K] (Д9К) and R = 300 Ω).

In the presence of at least one input of potential lower than the value corresponding to level 1, the triode is in saturation. The potential not differing from zero for ML3 should be considered a voltage not lower than 0.24 V.

The input state of ML3 is 5300 ± 300 Ω.

It is permissible to use module ML3 in devices in conjunction with ML2 and ML1. During calculation of the permissible number of modules in the load it is necessary to proceed from the input impedance of the load, i.e., in every case it is necessary to divide the minimum load impedance by the maximum permissible load.

The dimensions of the module are 25 × 21 × 14 mm.

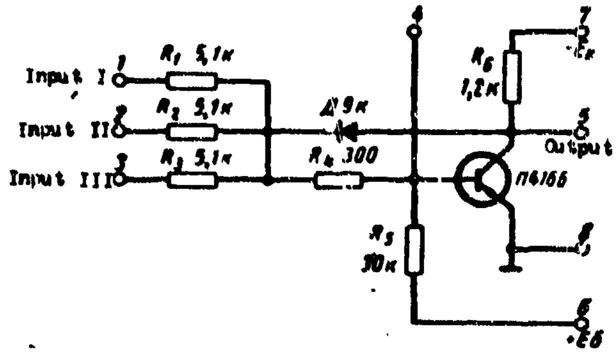


Fig. 78. The electrical schematic diagram of logic module ML3.

2. Auxiliary Elements

The time-setting stage ([KVz] (КВз)). The time stage of the kipp oscillator KVz is a passive element. It is a circuit consisting of a diode key and a time-setting circuit and can be used for construction of temporary delay units, temporary data storage units, etc.

The electrical schematic diagram of KVz is shown in Fig. 79.

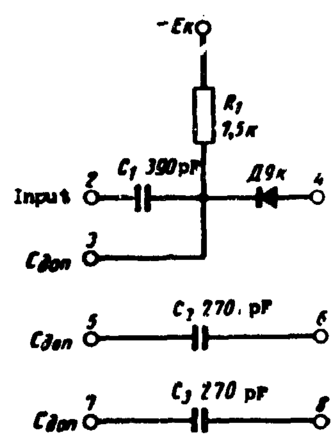


Fig. 79. The time-setting stage (KVz).

Increasing the time constant of the RC circuit to a value of the order of 4 μs requires using an additional capacitor, the value of which is determined by the formula

$$C_{don} = \frac{\tau}{4.5 \cdot 10^{9}} - C.$$

If the time constant <4 μs the value of the additional is **determined by the formula**

$$C_{доп} = \frac{\tau}{5{,}2 \cdot 10^{6}} - C,$$

where τ is in μs, and C is in farads.

As additional capacitances it is possible to use capacitors C_2 and C_3 of the time-setting stage. Inclusion in the layout of the kipp oscillator ([OV] (OB)), consisting of the KVz and two modules, is represented in Fig. 80.

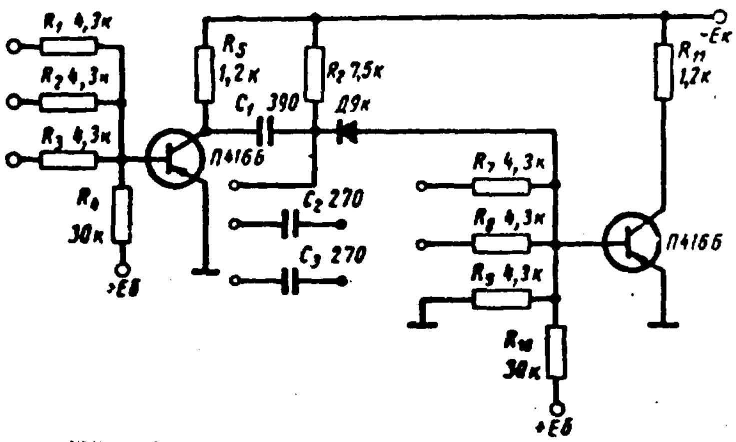


Fig. 80. The schematic diagram of the kipp oscillator (OV), consisting of the KVz and two modules.

The GSKTB recommends

a) ensuring the efficiency of the kipp oscillator consisting of KVz and ML1 (OV1) by using an additional capacitor not under 2400 pF connected in parallel with C_1 and C_2 of the time-setting stage KVz;

b) in the kipp oscillator composed of modules ML2 (OV2) using capacitance C_1 of stage KVz and in the kipp oscillator composed of modules ML3 capacitance C_2.

The OV is started by a positive drop from the logic module, which fulfills the function of a starting generator. The duration of the

interval of time of the existance of low negative potential (zero) at the output of the starting module should be greater than the duration of the shaping pulse. Otherwise OV is turned into a signal repeater supplied to the input of the starting module.

In the initial state the transistor of the module is open. On output OV there is a potential close to zero. Capacitor KVz is charged to the value of the collector voltage of the starting module the triode of which is in the cutoff mode. Upon the supplying of negative level to the input of the starting module the triode of the latter is opened, and the capacitor discharges on the following circuit: resistor R_1 of unit KVz, power supply, and open triode.

The positive voltage locks the triode, i.e., the triode of the module entering OV, is locked by the "zero" supplied to the input. Upon the achievement by the voltage at the capacitor of a level close to zero, the circuit is unitialized.

The working stage of pulse shaping after starting is determined by the time constant of the circuit (R_1C_2), and restore time is determined by the time constant R_2C_2 (R_2 is the resistance of the starting module).

The width of the pulse formed by the kipp oscillator with internal capacitor C_2 is equal to 1.5 ± 0.7 μs. The OV can form a pulse up to 200 μs wide.

The dimensions of the module are $26 \times 21 \times 14$.

Emitter repeater. The emitter repeater ([PE] (ПЭ)) is a current amplifier consisting of a powerful triode. It is used as an element with high load capacity in devices of reproduction of signals, for initial setting of circuits, for interrogation of parallel counters, and for other purposes.

The repeater triode with any signal at input remains in the linear mode, thanks to which it is possible to use PE in a wide frequency range.

The electrical schematic diagrams of PEm5 and PEm6 are shown in Fig. 81a and b.

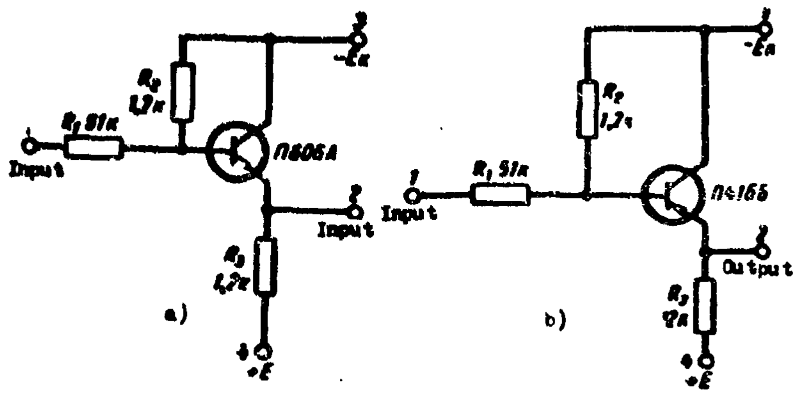


Fig. 81. Emitter repeaters: a) circuit PEm5; b) circuit PEm6.

Due to the fact that base current creates at the emitter junction a voltage drop different from the potential of the open buffer modules[2] u_0 in the direction of positive values, the buffer module is connected to the power supply E_K not through the collector resistor but through resistors R_1 and R_2. The collector current of the buffer module triode, flowing through resistor R_1, creates in it a voltage drop compensating for the withdrawal of voltage u_0. The buffer module can be used only with two inputs.

Emitter repeaters PEm5 and PEm6 are intended for operation under the following conditions (Table 66).

Table 66.

Conditions	ПЭм5	ПЭм6
Change of ambient temperature......	−60 to +70° C	−60 to +70° C
Voltage of power supplies..........	−6.3±0.63 v	−6.3 ± 0.63 v
Voltage of bias sources............	+ 6.3 ± 0.63 v	+6.3 ± 0.63 v
Frequency of work up to............	300 kHz	350 kHz
Resistive load not less than.......	72 Ω	400 Ω
Capacitive load not more than......	1000 pF	35 pF

The input impedance of PEm5 and PEm6 is 1000 Ω with a full load on module ML. For the modules of the load there can be used only two inputs.

The basic characteristics of PEm5 and PEm6 are represented in Table 67.

Table 67. Basic characteristics of potential modules and auxiliary elements of the SPE system.

No. in order	Characteristic	МЛ1	МЛ2	МЛ3	ПЭм6	ОВ2	ОВ3	ЭИ1	ЭИ2
1	Upper ambient temperature in °C.	+50	+70	+50	+70	+70	+50	+50	+70
2	Lower ambient temperature in °C.	–10	–60	–10	–60	–60	–10	–10	–60
3	Voltage of power supply in V.	–6,3±0,63	–6,3±0,63	–6,3±0,63	–6,3± ±0,63	–6,3± ±0,63	–6,3± ±0,63	–6,3± ±0,63	–6,3± ±0,63
4	Voltage of bias source in V.	+6,3±0,63	+6,3±0,63	+6,3±0,63	+6,3± ±0,63	+6,3± ±0,63	+6,3± ±0,63	—	—
5	Power drain in mW.	<50	<50	<50	<460	<50	<50	<540	<610
6	Load capacity in units.	4	3	4	10÷30	3	4	—	—
7	Potential of information zero in V.	–0,2	–0,05÷–0,2	–0,1÷–0,24	—	—	—	—	—
8	Potential of information 1 in V.	–2,0÷–3,7	–2,0÷–3,7	–2,8÷–3,5	—	—	—	—	—
9	Operating frequency counter circuit in kHz.	50	190	330	350	190	330	—	—
10	Width of signal front in μs.	8,1	1,5	0,8	1,2	0,6	0,5	—	—
11	Width of signal drop in μs.	1,7	0,2	0,3	0,35	0,2	0,3	—	—
12	Width of front delay in μs.	3,7	2,0	1,2	0,06	0,6	0,3	—	—
13	Width of drop delay in μs.	0,7	0,2	0,3	0,06	0,1	0,2	—	—
14	Pulse width in μs.	—	—	—	—	3,0	2,0	—	—
15	Permissible positive interference in V.	0,7	0,4	0,2	—	0,4	0,7	—	—
16	Permissible negative interference in V.	1,7	1,5	0,8	—	—	—	—	—

The dimensions of module PEm5 are 29 × 29 × 22.5 mm and of module PEm6 are 26 × 21 × 14 mm.

Indication elements. An indication element ([EI] (ЭИ)) is a static element with output to incandescent lamp [MN-2] (МН-2).

The indication element is produced in two variants.

Control of the indication element is carried out from ML, which as a result of the termination of the operation is set in state 1 for a long time.

The indication element consists of an emitter repeater and a final stage with deep negative feedback.

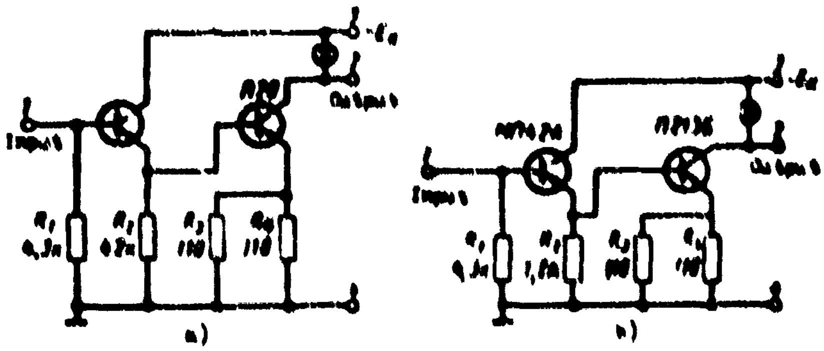


Fig. 82. Indication elements (EI).

The electrical schematic diagrams of EI1 and EI2 are represented in Fig. 82a and b, respectively.

The input impedance of EI is 2500 Ω.

The dimensions of module EI1 are 29 × 36 × 21 mm, and of module EI2 are 29 × 31 × 43.5 mm.

<u>Register element (ERg).</u> The register element is a passive element with three independent inputs intended for use in conjunction with any of the logic modules (ML) in the circuit of shift registers. The ERg elements are controlled via two resistance inputs by logic modules and a power repeater (PEm6).

In the initial state capacitors C_1 and C_2 are charged to the potentials of the collectors of starting modules. Diodes $Д_1$ and $Д_2$ are closed. At the time of income to the capacitive input of a negative shift pulse with a width determined by the type of the applied module, there occurs discharge of capacitors.

The capacitor connected by the resistors with the module collector which is in state 1 will be discharged almost to zero. The capacitor connected with the module collector which is in state 0 will be charged to the difference of potentials of the module collector and the potential of the emitter of the power repeater. Since level 0 is much lower than the amplitude of the shift pulse, the charge of the capacitor will change its sign. Upon completion of the action of the shift pulse on the resistance of the register element there is formed a positive pulse, which opens the corresponding diode and enters the

base of the triode of the load module. If the latter is in state 0, then the ERg signal will set the load module to state 1.

The electrical schematic diagram of ERg is shown in Fig. 83.

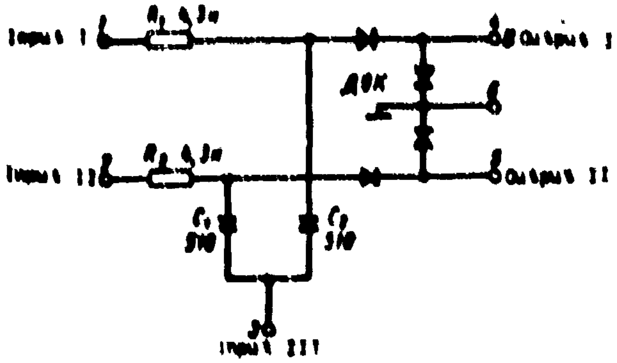


Fig. 83. The electrical diagram of the register element (ERg).

The ERg keeps its efficiency under the following conditions:

a) ambient temperature must very within the ranges:

+5 to +50°C during use with ML1;

-10 to +50°C during use with ML2 and ML3;

-60 to +70°C during use with ML2.

b) porosity of not less than 2 (frequency range 20-350 kHz);

c) pulse width of shift not less than 2 μs for modules ML2 and ML3 and not less than 15 μs for module ML1.

<u>Note</u>: ERg during work with ML1 requires application of additional 510 pF capacitances connected in parallel with the basic capacitor.

The input impedance of ERg on resistance inputs is not less than 4500 Ω.

The capacitive input of ERg in the register circuit is grounded through external resistor R_H, determined by the formula $R_н = \frac{324 \cdot 10^9}{4500 - 72n}$, where n is the number of bits of the register.

The dimensions of ERg are 26 × 21 × 14 mm.

The main characteristics of the potential elements of GSKTB are given in Table 67.

5.12. Model Potential-Pulse Elements of Industrial Automatics [50].

A. General Part

Model potential-pulse elements of a single series of [ET] (ЭТ) [Translator's Note: expansion of acronym unknown] developed with the participation of scientific colleagues of the Academy of Sciences of the USSR and specialists of various branches of the national economy; therefore, in this series there are considered various interests of a large circle of designer-developers, engineers, student-diploma candidates, and scientific colleagues of various [KB] (КБ) [Translator's Note: design-offices] and [NII] (НИИ) [Translator's Note: scientific research institutes] studying problems of designing devices and systems of industrial automatics, telemechanics, systems of centralized checking, control, signalling, measurements, etc.

The introduction into industry of potential-pulse elements of a single series of ET permits sharply increasing the reliability and speed of automatic control systems, expands the field of application of automated systems, and doubles or triples the productivity of labor in the manufacture of systems of industrial automatics.

With the introduction into industrial production of elements of a single series of ET, it ceases to be necessary to develop analogous elements and prepare them in individual order in numerous organizations, as was the case prior to 1965.

In the given division there are given a description of schematic diagrams, specifications and rules of connection of elements and also there are examined examples of construction of logic functions and basic cases of application of circuits in industrial automatics.

B. Types and Modification of Elements

The series of ET (Table 69) consists of 18 elements divided into 4 groups:

1) 6 logic elements;

2) 3 functional elements;

3) 4 time elements;

4) 5 outlet amplifiers.

<u>Logic elements</u>. The main active element of the series is the element realizing the "OR-NOT" function.

In the series provision is also made for a passive element realizing the "OR-AND" function. Furthermore, there are passive elements realizing "OR" and "AND" functions for pulse circuits and memory components.

<u>The functional elements</u> are intended for galvanic separation of circuits (coordinating element), formation of a discrete signal (relay element), and for comparison of the values of two voltages (null-balance device).

<u>The time elements</u> are intended for realization of time functions in pulse and potential circuits.

<u>The output amplifiers</u> are intended for transmission of instructions to servomechanisms with control powers up to 100 W.

The period of service of the elements does not depend on the number of switchings and is equal to 40 thousand hours with a probability of unfailing work of $P \geq 0.8$.

The elements ensure normal operation under the following conditions:

a) with deviation of supply voltage within the limits from -15 to +10% of its nominal value;

b) at an ambient temperature from -40 to +50°C;

c) at an ambient relative humidity of 98% and at a temperature of +40°C,

d) with vibrations in the frequency range from 5 to 20 Hz with acceleration to 4 g;

e) at impact loads with an acceleration of 15 g.

Transistor elements are reliable in operation, do not require regulation and adjustment during manufacture and exploitation, do not require removal, and can operate under unfavorable meteorological conditions.

The basic logic elements of the system can work at a switching frequency of up to 5 kHz. The working frequency of the remaining elements is shown in the table of technical data of the elements.

The elements are intended for work from discrete signals with two levels of voltages – the low level, conditionally designated 0, and the high level, conditionally designated 1.

Signal 0 should be not more than 0.9 V direct current, and signal 1 not less than 4.0 V direct current. The polarity of signals is negative.

The elements of series ET allow work with contactless and contact sensors and also with other controls, at the output of which there should be a signal of not less than 4.5 V of d-c voltage.

To increase reliability in the development of elements there were accepted considerable reserves for various components – transistors, diodes, resistors, and capacitors.

The supply voltage of the elements is -12 V or -25 V. Bias voltage is +6 V. The voltage rating on the external load of the elements is 24 V direct current.

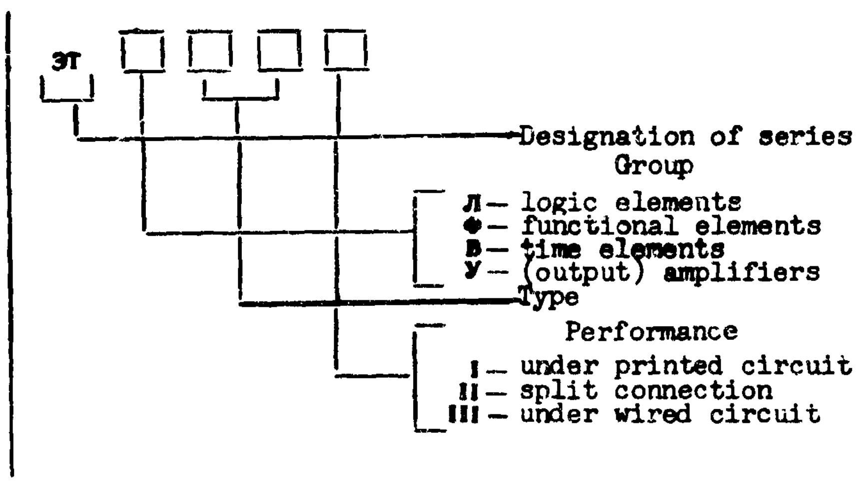
Table 69. Series of elements ET.

No. in order	Type of element	Group of element	Assignment of elements
1	ЭТ-Л01		The double "OR-NOT" rheostat-transistor circuit realizes the universal logic functions $y=\overline{a+b+c}$
2	ЭТ-Л02		The "OR-NOT" diode attachment realizes the logic functions $y=a+b+c+d+e+h$; $y=a\cdot b\cdot c\cdot d\cdot e\cdot h$
3	ЭТ-Л03		Low-power (computing) flip-flop. It is used in the circuits of counters, resistors, etc., and also as "Memory."
4	ЭТ-Л04	Logic	High-capacity (computing) flip-flop. It is used in branched circuits of matrix encoders and decoders and also as "Memory" during work on a relay or signal lamp.
5	ЭТ-Л05		The double potential-pulse cell. Composition of "OR" and "AND" pulse circuits and reproduction of inputs of the ET-L03 element.
6	ЭТ-Л06		The same, and also reproduction of inputs of ET-L04 element.
7	ЭТ-Ф01		Coordinating input element. Galvanic separation of electric circuits.
8	ЭТ-Ф02	Functional	Relay element. Conversion of continuous changes of input voltages into a discrete signal of the assigned level (discriminator of amplitudes).
9	ЭТ-Ф03		Null-balance device. Comparison of two voltages with respect to value.
10	ЭТ-В01		Ternary RC circuit. Application in circuits for delay of pulses and also as a filter.
11	ЭТ-В02	Time	Double transistor delay for construction of delay lines, kipp oscillators, multivibrators, etc.
12	ЭТ-В03		Time delay up to 10 s with regulator within limits from 0.5 to 10 s.
13	ЭТ-В04		Time delay up to 100 s with regulation within limits from 9 to 100 s.

Table 69. (Cont'd)

No. in order	Type of element	Group of element	Assignment of elements
14	ЭТ-УО1		A binary coordination amplifier for increasing the load capacity of logic circuits for switching on of signal lamps (at output up to 40 mA at 12 V).
15	ЭТ-УО2		A 3 W binary output amplifier; 125 mA. Switching on of EMU and MU windings, intermediate relays, and signal lamps.
16	ЭТ-УО3	Amplifiers	Output amplifier of power up to 10 W; 420 mA. Switching on of EMU and MU windings, intermediate relays, and signal lamps.
17	ЭТ-УО4		A 30 W, 1.25 a output amplifier. Switching off of windings of magnetic amplifiers, contactors, solenoids, and others.
18	ЭТ-УО5		A 100 W, 4.2 a output amplifier. Switching on of windings of magnetic amplifiers, powerful contactors, solenoids, and others.

The model designation of elements is composed in the following way:



Note: Performance of element is characterized by appearance and is not shown in designation on element. Type of performance is recorded only in the documentation, for example: ET-L03-1.

Designations: ЭТ-Л01 = ET-L01, ЭТ-Ф01 = ET-F01, ЭТ-В01 = ET-V01, ЭТ-У01 = ET-U01, EMU = ЭМУ, MU = МУ.

Structurally the elements are shaped in the form of modules. Semiconductors and other completion articles are mounted on laminated-insulation plate with a printed circuit.

For protection from the influence of the environment and also for the possibility of bracing elements on a common plate, plates with elements mounted on them are flooded with a compound on an epoxy base and are placed in a carbolite housing with a cover. The construction cannot be dismounted or repaired.

By method of connection to external wiring the elements are produced in three performances:

performance I — with cylindrical leads under soldering to plates with printed circuitry;

performance II — with printed leads under plug connector;

performance III — with platelet leads under wired circuitry.

The marking of the leads of elements is numerical from 1 to 18. Voltage of +6 V is lead out to the 14-th lead; 0 to the 15-th; -12 V to the 16-th; -24 V to the 17-th lead.

C. Logic Elements

a) Element ET-L01

Element ET-L01 (Fig. 112) has two independent "OR-NOT" circuits each of which has three inputs (input impedances 1500 Ω) and one inverse output. The element realizes the function $y = \overline{a \vee b \vee c}$.

The parameters of element ET-L01

Supply voltage in V....................................	+6; -12
Consumption of current in mA..........................	2 × 15
Load resistance in Ω..................................	2 × 820
The input impedance of the first input in kΩ.............	1.5

Working frequency of switchings in kHz	5.0
Level of voltages in V.	
input signal 0 with three connected inputs	0.5
input signal with one connected input	0.95
input signal 1 with any connection of inputs	12
output signal 0	0.15
output signal 1	4-12

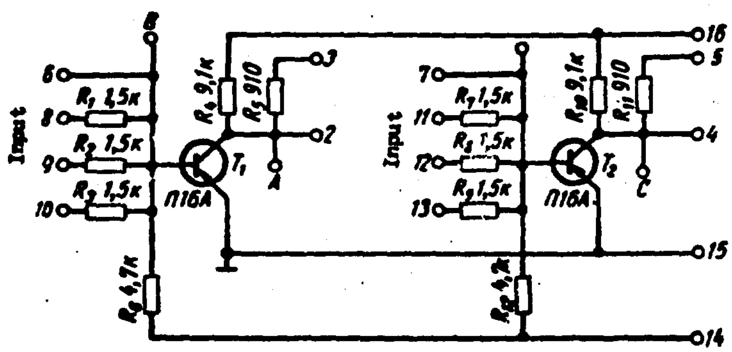


Fig. 112. The electrical schematic diagram of element ET-L01.

In the absence of signal at all inputs the transistor is closed, and at its output there is negative potential (accepted in the system as 1).

If at least one of the inputs is supplied with a signal equal to 1, the transistor is opened, and at the output the signal vanishes.

During the work of the element to the input of other elements (besides element ET-L02, realizing function "AND") leads 3 and 5 must be connected with lead 16. Moreover, in the elements there are used both collector resistors (9.1 kΩ and 910 Ω), connected in parallel.

During the work of element ET-L01 to the input of element ET-L02 (realizing function "AND") in the collector circuit there is used one 9.1 kΩ resistor, which ensures reverse bias of the diodes of attachment "AND."

With the help of element ET-L01 it is possible to realize the following logic functions:

1. The "OR" function (Fig. 113a). The signal appears at the output when there is a signal at at least one of the inputs:

$$x = a_1 \vee a_2 \vee a_3.$$

2. The "AND" function (Fig. 113b). The signal appears at the output only if there are signals at all inputs:

$$x = a_1 \cdot a_2 \cdot a_3.$$

3. The "NOT" function (Fig. 113c). In the presence of a signal at the input the signal is absent at the output; the signal appears at the output when the signal vanishes at the input:

$$x = \bar{a}.$$

4. The "AND-NOT" function (Schaeffer operation) (Fig. 113d). The signal is absent at the output only if there are signals at all three inputs:

$$x = \overline{a_1 \cdot a_2 \cdot a_3}.$$

5. The "OR-NOT" function (Pierce operation) (Fig. 113e). The signal is absent at the output when there is a signal at at least one of the three inputs:

$$x = \overline{a_1 \vee a_2 \vee a_3}.$$

6. The "Inhibit" function (Fig. 113f). The signal at the output appears simultaneously with the signal at input "a" if the signal is absent at the inhibit input "b." In the presence of signal at the inhibit input "b" the signal is absent at the output.

7. The "Memory" function (Fig. 113g). When the signal is supplied to input "a" (switching on of memory) the signal appears at the forward output and disappears at the inverse output. This state is preserved until the signal is supplied to input "b" (switching off of memory). After the supplying of power the state of the circuit is arbitrary.

8. <u>The "unequivalence" (unequivalentness) function</u> (Fig. 113h). The signal at the output exists only if the signals at inputs "a" and "b" do not match.

9. <u>The "Implication" function</u> (Fig. 113i). The signal at the output is absent only if there is a signal at input "a" and the signal at input "b" is absent.

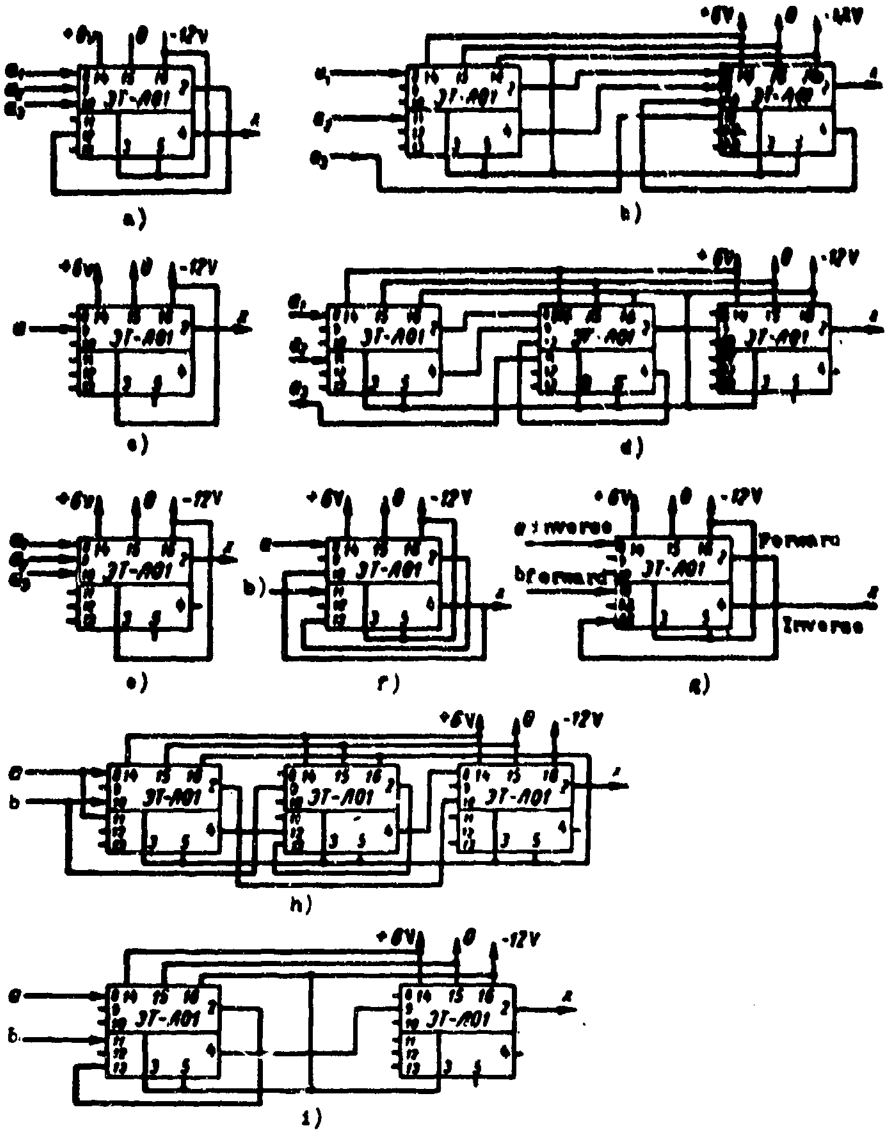


Fig. 113. Logic functions realized with the help of element ET-L01: a) realization of "OR" function $(x = a_1 \vee a_2 \vee a_3)$; b) realization of "AND" function $(x = a_1 \cdot a_2 \cdot a_3)$; c) realization of "NOT" function $(x = \overline{a})$; d) realization of "OR-NOT" function — Schaeffer operation $(x = \overline{a_1 \cdot a_2 \cdot a_3})$; e) realization of "OR-NOT" function — Pierce operation $(x = \overline{a_1 \vee a_2 \vee a_3})$; f) realization of "Inhibit" function; g) realization of "Memory" function; h) realization of "Unequivalence (unequivalentness) function; i) realization of "Implication" function.

b) The element of type ET-LO2

Element ET-LO2 (Fig. 114) (the universal diode attachment) is a set of diodes of type [D9D] (Д9Д) the leads of which are not connected. With the help of external connections of diode leads an "OR" circuit or an "AND" circuit can be realized. The element allows obtaining simultaneously up to three "OR" circuits, up to two "AND" circuits, and a combination of "OR" and "AND" circuits with a total of up to six inputs.

Parameters of the element when the "AND" circuit is switched on

Supply voltage in V	-12
Load resistance in Ω	2400, 1200, 800
Output voltage in the absence of signal at the input of the element in V	≤0.65
Consumption by the element of current in the presence of signals at the inputs in mA	3, 6, 9
Consumption by the element of current in the absence of signals at the inputs in mA	5, 10, 15
Working frequency in kHz	Up to 5

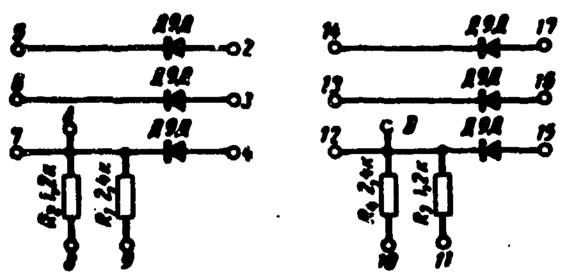


Fig. 114. The electrical schematic diagram of a universal diode attachment for the realization of an "OR" circuit or an "AND" circuit.

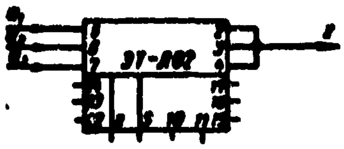
Examples of realization of logic functions with the help of an ET-LO2 element.

1. Realization of an "OR" function (Fig. 115a).

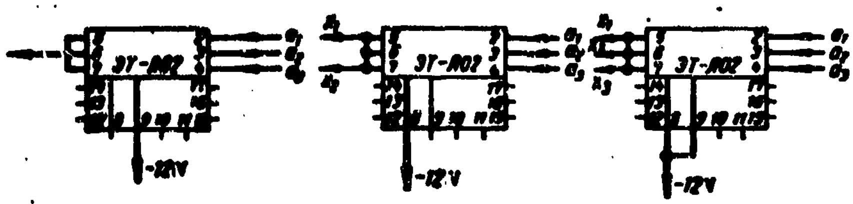
2. Realization of an "AND" function (Fig. 115b).

3. Connection of a passive "OR" circuit to the output of a passive "AND" circuit (Fig. 115c).

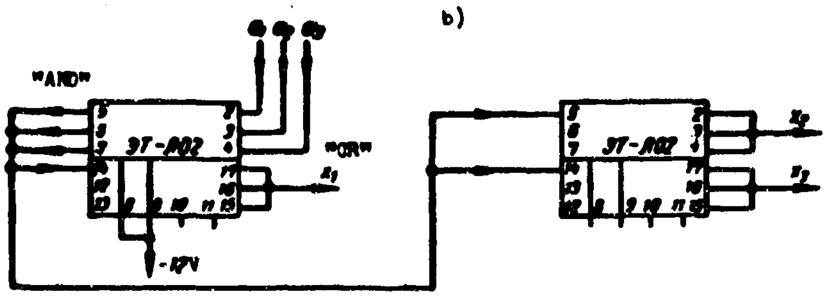
The output of the passive "OR" circuit is not allowed to be connected to the input of the passive "OR" and "AND" circuits. Neither is the output of the passive "AND" circuit allowed to be connected to the input of the passive "AND" circuit.



a)



b)



c)

Fig. 115. Examples of the realization of logic functions with the help of an ET-L02 element; a) realization of "OR" function; b) realization of "AND" function; c) connection of passive "OR" circuit to output of passive "AND" circuit.

c) Examples of realization of logic functions in the combination of ET-L01 and ET-L02

1. The "Equivalence" function (Fig. 116a). The signal exists at the output only if input signals are absent at both inputs simultaneously.

2. One of the variants of connection of ET-L01 to the input of ET-L02 realizing the "AND" function (Fig. 116b).

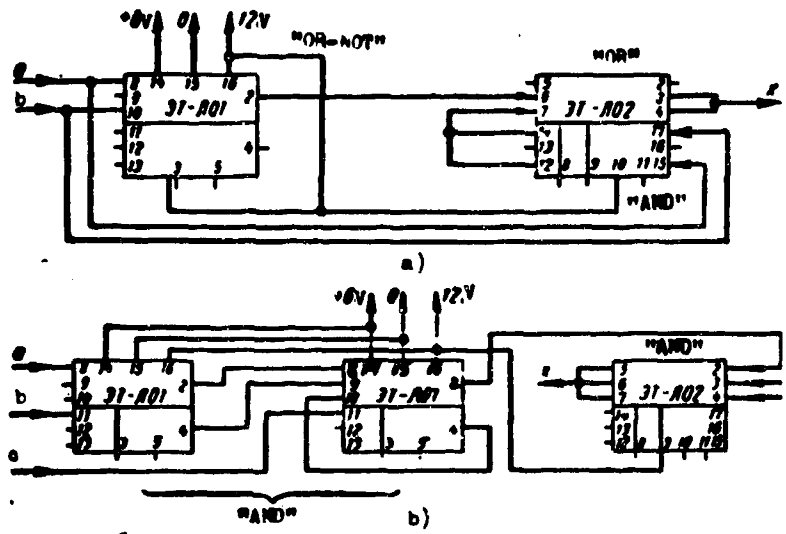


Fig. 116. Examples of realization of logic functions in the combination of elements ET-L01 and ET-L02. a) realization of the "Equivalence" function; b) variant of connection of ET-L01 to the input of ET-L02 realizing the "AND" function.

d) Element ET-L03

Element ET-L03 (Fig. 117) (a low-capacity flip-flop) is a switching device having two stable states. Element ET-L03 can be used as a frequency divider, a computing cell, as "Memory," etc.

The parameters of element ET-L03

Supply voltage in V	+6, -12
Consumption of current in mA	15
Amplitude of starting pulse in V	4-7
Width of starting pulse in ms	0.1
Starting current in mA	5
Current of external load in mA:	
nominal	15
maximum	25

Level of output voltage in V:

  signal 0 .... 0.2

  signal 1 .... 4.5-6.0

Working frequency in kHz 5

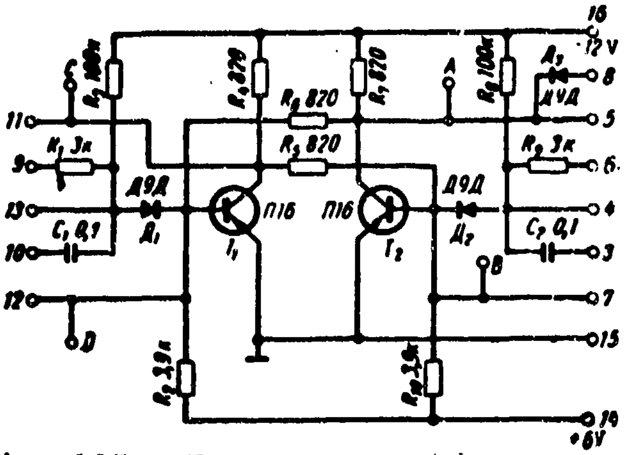


Fig. 117. The electrical schematic diagram of the low-capacity flip-flop (the ET-L03 element).

Elements ET-L03 allow work when the circuit is connected with the general computing input. Leads 3 and 10 and the circuit are connected with the divided inputs (leads 6 and 5 as well as 9 and 11 are connected).

To initialize simultaneously all the cells of the scalers leads 8 of all elements have to be united and briefly fed zero potential (Fig. 118).

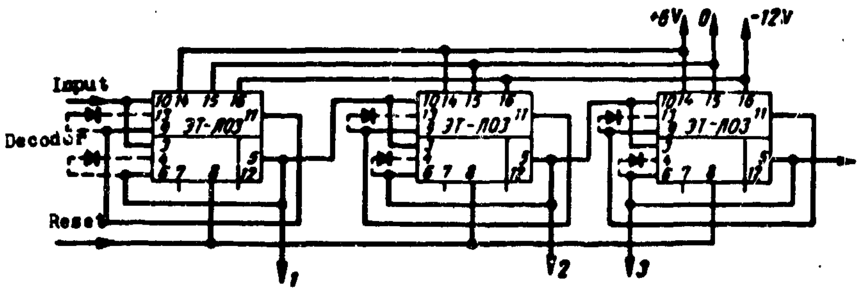


Fig. 118. An example of the construction of a binary integrating counter consisting of ET-L03 elements.

e) An example of construction of a binary integrating counter and the principle of its operation

When potential is fed to the "Reset" bus through diode $Д_3$ (Fig. 117) the potential of the collector of transistor T_2 also takes on zero value. The potential at the base of transistor T_1 takes on a positive value close to zero, and transistor T_2 is kept in the open state after the removal of zero potential from the "Reset" bus.

On the collector of the closed transistor T_1 there is negative potential

$$u_к = \frac{u_{пит} R_5}{R_3 + R_5} = \frac{u_{пит}}{2},$$

and at the base there is positive close to zero. The difference of these potentials is applied to diode $Д_1$ (through the collector, lead 11, lead 9, and resistor R_1) and locks it.

The closed diode does not let pass positive signals lower than $u_к$, and presents for them an opened key. Therefore, any positive signal (interference) less than $u_к$ in amplitude entering the input of the circuit cannot get to the base of the closed transistor T_1. Diode $Д_2$, connected with the base and with the collector of the saturated transistor T_2, is open since from both sides of the diode there is applied almost identical potential equal to the potential of the ground. Therefore, diode $Д_2$ is a closed key and easily lets pass to the base of the saturated transistor T_2 positive signals entering the input of the circuit.

Thus, the examined diode key sends positive signal only to the base of the saturated transistor and does not pass it to the base of the closed transistor. Thereby there is created the condition for locking saturated transistor T_2 and simultaneously there do not worsen the conditions of unlocking the transistor closed earlier T_1, i.e., the diode key facilitates the condition of reversing of the flip-flop.

If the input of the system is fed a signal of negative polarity, then capacitance C_2 will be charged on the circuit: ground bus, emitter-collector T_2, lead 5, lead 6, resistor R_9, capacitance of plate of capacitor C_2 from the side of tape 4 and from the side of tap 3 (a positive charge is stored on the plate from the side of tap 4, and a negative one from the side of tap 3).

At capacitance C_1 there is not stored a charge since transistor T_1 is closed, and from both sides of capacitance C_1 there are applied identical negative potentials. Thus, there is charged only the capacitance, which is connected with the saturated transistor. This permits storing the state of the flip-flop during the throwing over the flip-flop to ensure the development of the regenerative process in the necessary direction.

After the supplying to the system input of a signal of zero potential, the plates of capacitors C_1 and C_2 from the side of taps 3 and 10 also take on zero value.

Capacitance C_2 is connected through diode Д$_2$ to the base junction-emitter by positive potential to the base.

The discharge of capacitance C_2 occurs through resistors R_5 and R_9. In the first moment through the discharge of capacitance C_2 minority carries accumulated in the region of the base are resorbed through the emitter junction, and transistor T_2 is locked.

Consequently, the part of the energy accumulated in capacitance C_2, after the entering of the input signal is expended locking the saturated transistor, which ensures even flipping of the flip-flop.

With the supplying to the system input of a signal of negative polarity the flip-flop is flipped, after which the charging of capacitance C_1 begins. Capacitance C_2 is almost not charged.

When the input is fed a signal of zero value, capacitance C_1 discharges to the base of a saturated transistor T_1, and the flip-flop returns to its initial state.

The distinctive peculiarity of the flip-flop circuit is the fact that the process of flipping the flip-flop precedes the process of preparation, when the corresponding storage or accelerating capacitance is charged. For this reason the repetition rate of the input pulses is limited by the time of charging of the capacitance through resistor R_1 or R_9. This determines the relatively low working frequency of the flip-flop. To expand the working range to 10 kHz resistors R_1 and R_9 must be shunted by diodes $Д_{ш}$, as is shown by the dotted line in Fig. 113.

In the flip-flop with separate inputs the process of preparation and operation occurs analogously, the only difference being that signals alternately enter the corresponding individual inputs.

The load to the flip-flop can be connected both in series with the transistor through the diode attachment and in parallel with the transistor.

It is preferable for the load to be connected in series since this method provides high load capacity and noise immunity of the flip-flop.

The triggers in the counting circuits can be reset by one reset pulse both through the collector and through the base. During reset ground potential is supplied to the flip-flop output.

The flip-flop from the other elements can be controlled by additional base leads 7 and 12.

In order to consider the pulses of negative polarity it is necessary to supply signals to the input of the examined circuit through the "AND-NOT" logic cell.

Resistors R_3 and R_8 (100 kΩ) serve to reverse the bias of the diodes in those cases in which resistors R_1 and R_9 are not connected with the collector and are used as additional flip-flop inputs for the realization of various logic functions.

f) Element ET-L04

Element ET-L04 (high-capacity flip-flop) is intended for work to relay coils, signal lights, in branched chains of a matrix decoder, and others.

The parameters of the ET-L04 element

Supply voltage in V	+6, -25
Consumption of current in mA	120
Amplitude of starting pulse in V	4-20
Width of starting pulse in ms	1.0
Starting current in mA	15
Current of external load in mA:	
nominal	70
maximum	100
Levels of output voltage in V:	
signal 0	0.15-0.5
signal 1	1.0-25
Working frequency in kHz	Up to 0.5

The schematic diagram of the high-capacity flip-flop (Fig. 119) differs from the circuit of the low-capacity flip-flop (Fig. 117) and is a cross connection of two inverters through diode connections. This permits excluding the flow of base current through the load and increases current and voltage drop in the load. If in the circuit of the low-capacity flip-flop because of the equality of resistors R_4 and R_5 the current drop and the voltage drop in the load is equal to $\frac{u_{\text{пит}}}{2}$, then in the circuit of the high-capacity flip-flop due to the presence of the diode connection the base current of transistor T_1 flows through the circuit (resistors R_3 and R_6) and does not get to the load of the other transistor T_2. Therefore, in the load there takes place a full drop of current $I_{КО}-I_{КН}$ and of voltage $0-u_{\text{пит}}$. This ensures normal work of the relay or lamp, included in the circuit of the collector of the transistor. The flip-flop is controlled by signals from other elements through the potential-pulse cells analogously to the way this is done for the low-capacity flip-flop.

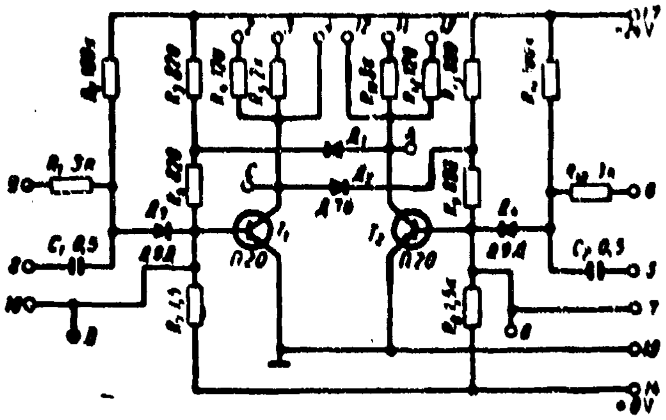


Fig. 119. The electrical schematic diagram of the high-capacity flip-flop (element ET-L04).

When transistor T_1 is open, zero potential from its collector is supplied through diode $Д_2$ to the base circuit of the other transistor T_2 and closes it. Analogously to this when transistor T_2 is open, the input of transistor T_1 is fed a positive signal through diode $Д_1$, and transistor T_1 is closed. Diodes $Д_1$-$Д_4$ in the flip-flop circuit fulfill the role of an ordinary valve, and no special requirements are placed on it. Resistors R_2 and R_{14} (100 kΩ) permit reversing diode bias, limiting the charge of the capacitors (C_1 and C_2) and the passage of interferences to the base of the open transistor. Working frequency is up to 500 Hz.

Fig. 120a gives an example of inclusion of a relay in the circuit of element ET-L04. If the coil of the relay is included in only one arm of the flip-flop then in the opposite arm it is desirable to connect resistor R_{11} = 2 kΩ, having connected lead 17 with lead 11.

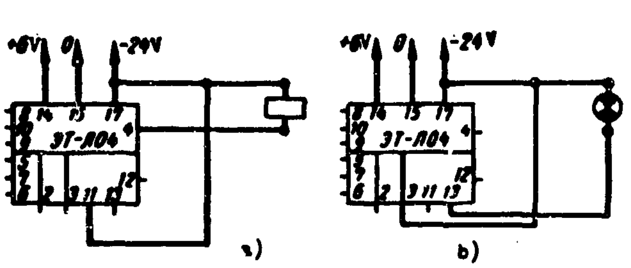


Fig. 120. Examples of inclusion of a relay and a lamp in the circuit of element ET-L04: a) inclusion of relay; b) inclusion of lamp.

Fig. 120b gives an example of inclusion of a signal lamp in the circuit of element ET-L04. The lamp is connected is series with resistor R_{12} = 120 Ω. When the lamp is included in one arm it is necessary to include resistor R_{13} = 2 kΩ in the other arm.

g) Elements ET-L05 and ET-L06

Elements ET-L05 (Fig. 121a) and ET-L06 (Fig. 121b) (potential-pulse cells) are intended for conversion of potential signals into pulse signals, for realization of pulse logic circuit, and for operation in conjunction with logic elements of types ET-L03 and ET-L04.

Parameters of elements ET-L05 and ET-L06

	ET-L05	ET-L06
Supply voltage in V...................................	-12	-25
Working frequency of switchings in kHz...............	5.0	0.5
Input impedance (dynamic) in kΩ......................	3.0	3.0
Amplitude of input pulse in V........................	≤12	≤12
Width of input pulse in ms...........................	300	300
Output resistance in kΩ..............................	≤0.1	≤0.1

For conversion of the potential signal into a pulse signal lead 3 is constantly fed a zero potential, and at the input (lead 2), the potential of the signal alternately varies from zero to negative value $-U_K$.

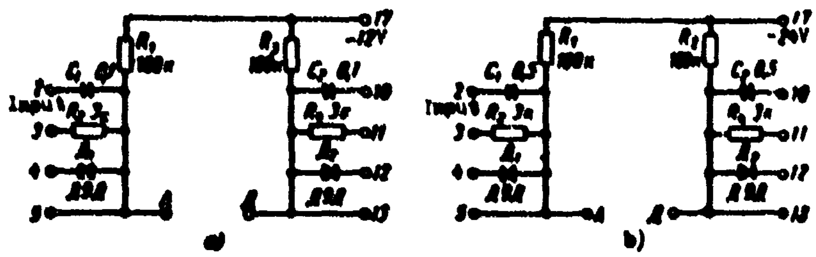


Fig. 121. Electrical schematic diagrams of potential-pulse cells: a) potential-pulse cell (element ET-L05); b) potential-pulse cell (element ET-L06).

Then in the presence at the input of negative potential capacitance C_1 through resistance R_2 during the time Δt = kRC is charged and at

the right plate of the capacitance there is stored a positive charge, while at the left one a negative charge is stored.

After the charge of the capacity during the supplying to the input of zero potential capacitance C_1 starts to discharge through load R_H and resistance R_2 (Fig. 122).

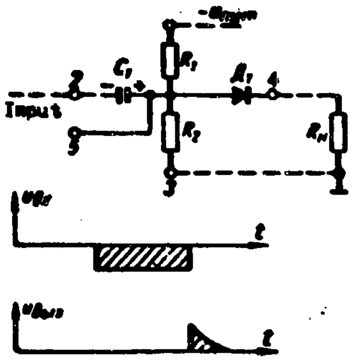


Fig. 122. The process converting potential signal into pulse signal.

At the output we obtain pulses of positive polarity, with the help of which it is possible to control the locking of the flip-flop of other cells.

Resistor R_1 = 100 kΩ is connected to the negative potential of the source and is used for reverse bias of the diode, which limits the passage of interferences from the inputs of the circuit to its output and increases noise immunity. Application of potential-pulse cells permits considerably reducing the number of transistors in circuits of automatics and telemechanics, since controlling triode cells through potential-pulse cells makes it unnecessary to use intermediate amplifiers.

D. Functional Elements

1. Element ET-F01

Element ET-F01 (coordinating element) is intended for coordination of parameters of galvanically isolated sensors and system elements.

Parameters of element ET-F01

Voltage of alternating current in V....................	220
Voltage of direct current in V.........................	12, 110, 220
Consumption of current in mA:	
on direct current circuit............................	≤ 15
on alternating current circuit.......................	≤ 50
Control current in mA..................................	≤ 15
Output voltage when $R_{BX} = 1.5$ kΩ in V...................	4.5
Voltage of output voltage pulsations in %..............	≤ 10
Delay time of output signal in s.......................	≤ 0.1

The element can be used also in case of coordination of parameters of the separate components of the system, when resistance coupling must be replaced by magnetic coupling.

Element ET-F01 ensures transmission of switching signals of transistor elements from 110 V and 220 V direct current sources of signals and 220 V alternating current sources.

Element ET-F01 is represented in Fig. 123a and b, where it is given in combination with other elements.

At the input of the "OR-NOT" transistor logic element (Fig. 123a) the input signal appears upon the pressing of button K, included in the field winding circuit. The current and, consequently, the field ampere-turns become equal to zero, and the alternating current is transformed from the primary winding connected to the 220 V network to the secondary (output) winding. After rectification and smoothing the current gets to the input of the transistor element.

In the second variant the field winding is de-energized. Upon the pressing of button K the primary winding is connected to the 220 V alternating current network and in the secondary (output) winding of the transformer there is transformed the voltage, which after rectification and smoothing gets to the input of the transistor element.

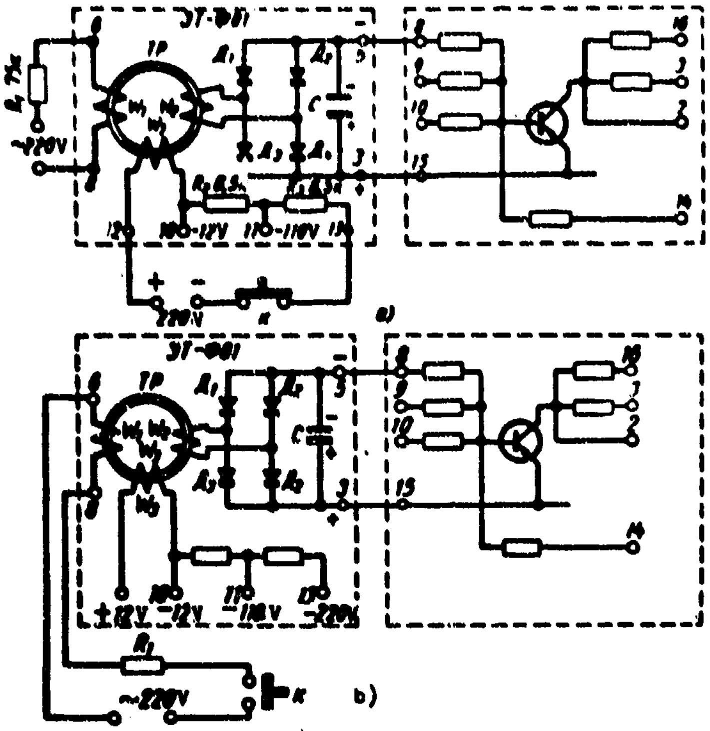


Fig. 123. Examples of the practical application of ET-F01 elements: a) comtrol by direct current (first variant) b) control by direct current (second variant).

b) Element ET-F02

Element ET-F02 (the relay element) possesses the relay characteristic "input-output" and is intended for conversion of smoothly variable input voltage into discrete output signal of the established level (Fig. 124a).

The given diagram is an assymmetrical flip-flop built on the basis of a two-stage d-c amplifier with positive feedback.

The characteristic of $u_{вых} = f(u_{вх})$ is shown in Fig. 124b).

Through the introduction of feedback there is achieved an avalanche-type process of building up of output signal with increase of input signal to a certain value.

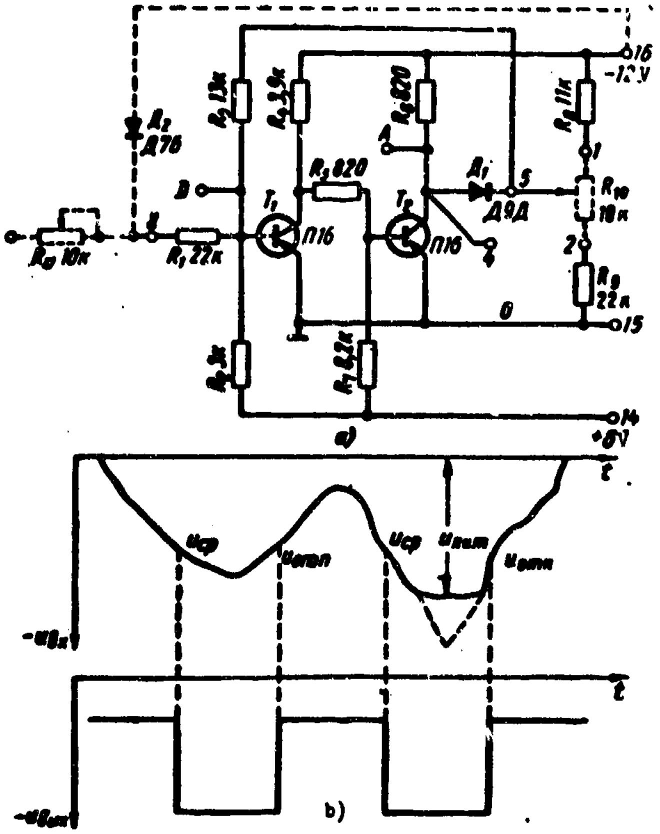


Fig. 124. The electrical schematic diagram of relay element ET-F02: a) diagram of element; b) diagram of work of element

The feedback circuit is connected to divisor R_8, R_9, R_{10}, which during the operation of the relay is untied from the rest of the circuit by diode $Д_1$. To lock the diode the voltage of the feedback circuit must be lower than the voltage at the load. With such a circuit the feedback current does not depend on the value of the load.

The voltage of the operation of the element is regulated within wide limits by the change of input impedance R_{11}.

The parameters of element ET-F02

Supply voltage in V.	+6, -12
Consumption of current in mA.	15
Range of regulation of voltage in V.	4-20

Load resistance in Ω	320
Input impedance in kΩ	2.0
Response time in ms	≤ 1
Working frequency in kHz	5

During the work of the element in systems where there are possible considerable bursts of input voltage, it is necessary to limit the amplitude of the latter, which is achieved with the help of diode $Д_2$. This diode limits the input signal in that case in which the latter exceeds the value of supply voltage -12 V. In this case diode $Д_2$ is opened, and the surplus of output voltage drops on potentiometer R_{11}.

The relay element is designed in such a way that its output is to be connected to not more than three "OR-NOT" circuits (not more than three 1500 Ω inputs).

c) Element ET-F03

Element ET-F03 (null-balance device), represented in Fig. 125a, is an element comparing the values of two direct current voltages. Input 1 and input 2 are fed comparable voltages. Input 1 (lead 7) is fed a checked voltage, and input 2 (lead 11) a reference voltage.

The main center of the null-balance device is the blocking-generator. The transistors T_1 and T_2, working in diode conditions, switch on the circuit of the positive (W_1) or negative (W_2) feedback of the blocking-generator.

With excess u_{BX1} over u_{BX2} transistor T_1 is open, and transistor T_2 is closed. The negative feedback winding (W_1) is switched on, and the blocking-generator does not operate.

If $u_{BX2} > u_{BX2}$, transistor T_2 is opened, and transistor T_1 is locked, which leads to appearance of relaxation oscillations through the switching on of the positive feedback winding (W_2). The blocking-generator starts to generate.

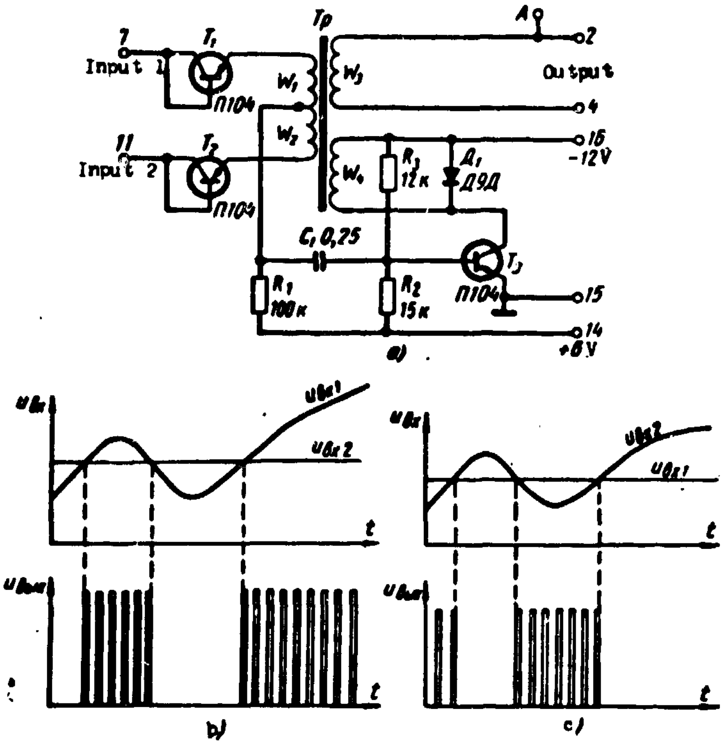


Fig. 125. The electrical schematic diagram of the null-balance device (element ET-F03): a) the circuit of the null-balance device; b) the diagram of work of the null-balance device for the case of connection of reference voltage at input 1 (leads 7 and 14), and of checked voltage to input 2 (leads 11 and 14); c) the diagram of work of the null-balance device for the case of connection of reference voltage to input 2 (leads 11 and 14) and of checked voltage to input 1 (leads 7 and 14).

Transistors in the diode mode and possessing low forward resistance are used to obtain steeper and more identical diode characteristics. Furthermore, the application of transistors improves the sensitivity and stability of the null-balance device. To improve sensitivity still more the median point of the feedback windings is connected to the bias source through resistor R_1 = 100 kΩ.

Oscillations appear at the output of the blocking-generator when the voltages are equal with an accuracy of 50-100 mV. The frequency at the output of the blocking-generator is about 100 Hz.

The width of the pulses $T_{ИМП}$ = 200-250 μs.

Figure 125b shows the diagram of work of the null-balance device for the case of connection of the reference voltage to input 2 (leads 11 and 14), and the checked voltage to input 1 (leads 7 and 14). For this case relaxation oscillations at the output of the element appear when the checked voltage exceeded the reference voltage.

Figure 125c gives the diagram of work of the null-balance device for the case of connection of reference voltage to input 1 (leads 7 and 14) and of checked voltage to input 2 (leads 11 and 14). Relaxation oscillations appear at the output of the element when the reference voltage exceeds the checked voltage.

The parameters of element ET-F03

Supply voltage in V..	+6; -12
Consumption of current (mean value) in mA....................	≤ 20
Input voltage in V..	≤ 20
Sensitivity in mV..	≤ 50
Internal resistance (dynamic) in kΩ..........................	≥ 0.1
Response time in ms..	≤ 10
Amplitude of output voltage in V............................	≥ 10
Width of output pulse in ms....................................	≥ 0.1
Internal resistance in kΩ..	≤ 1.0

E. Time Elements

a) Element ET-V01

The schematic diagram of element ET-V01 (triple RC circuit) is presented in Fig. 126.

The parameters of element ET-V01

Input impedance in kΩ..	1.5
Time constant of charge in ms............................	75 ± 25%

Such a circuit can be used as an integrating network for delaying a signal, as a differentiating circuit, and as a filter of high-frequency interferences.

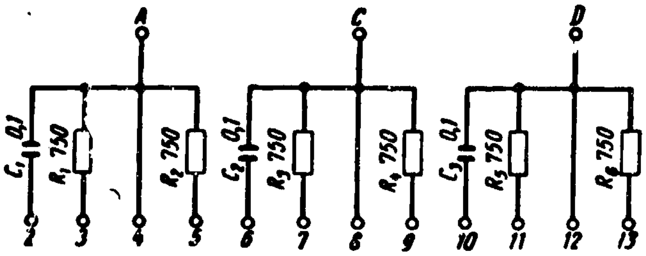


Fig. 126. The electrical circuit of the time element (element ET-V01) — triple RC circuit.

When necessary the time constant of the RC circuit can be increased by way of connection to median points of circuit A, C, D of external capacitance.

The RC circuit can be used in logic circuits, for example, in those cases, in which the signal from the output of the pulse-potential coincidence circuit must enter the input of that potential element which controls the operation of the given coincidence circuit.

In this case it is necessary to delay the control signal entering the potential input of the coincidence circuit until the pulse is finished at the pulse input in order to prevent the passage of the spurious signal to the second input.

For this purpose at the potential input of the coincidence it is possible to set a delaying RC circuit which will ensure the assigned work of the circuit.

b) Element ET-V02

Element ET-V02 (transistor delay) is an inverter with capacitances at the input (Fig. 127), which ensures the obtaining of a time delay of the signal when a zero signal is supplied to the input.

The parameters of element ET-V02

Supply voltage in V	-12
Consumption of current in mA	6
Load impedance in kΩ	2.4
Delay time in μs	20, 300, 700
Utilization factor of capacitance in μF/s	150
Collector current in mA:	
nominal	5
maximum	15
Amplitude of input voltage in V	Up to 12
Output voltage of signal 0 in V	0.15
Output voltage of signal 1 in V	4.5-12

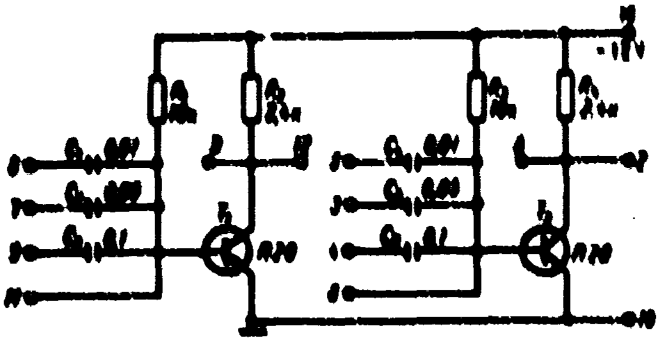


Fig. 127. The electrical circuit of element ET-V02 (transistor delay).

Element ET-V02 is used in circuits of automatics and telemechanics in the following cases:

a) for limitation of the duration of action of the signal (Fig. 128a);

b) in circuits of multivibrators (Fig. 128b);

c) in circuits of delay lines (Fig. 128c);

d) in diagram circuits of kipp oscillator (Fig. 128d), etc.

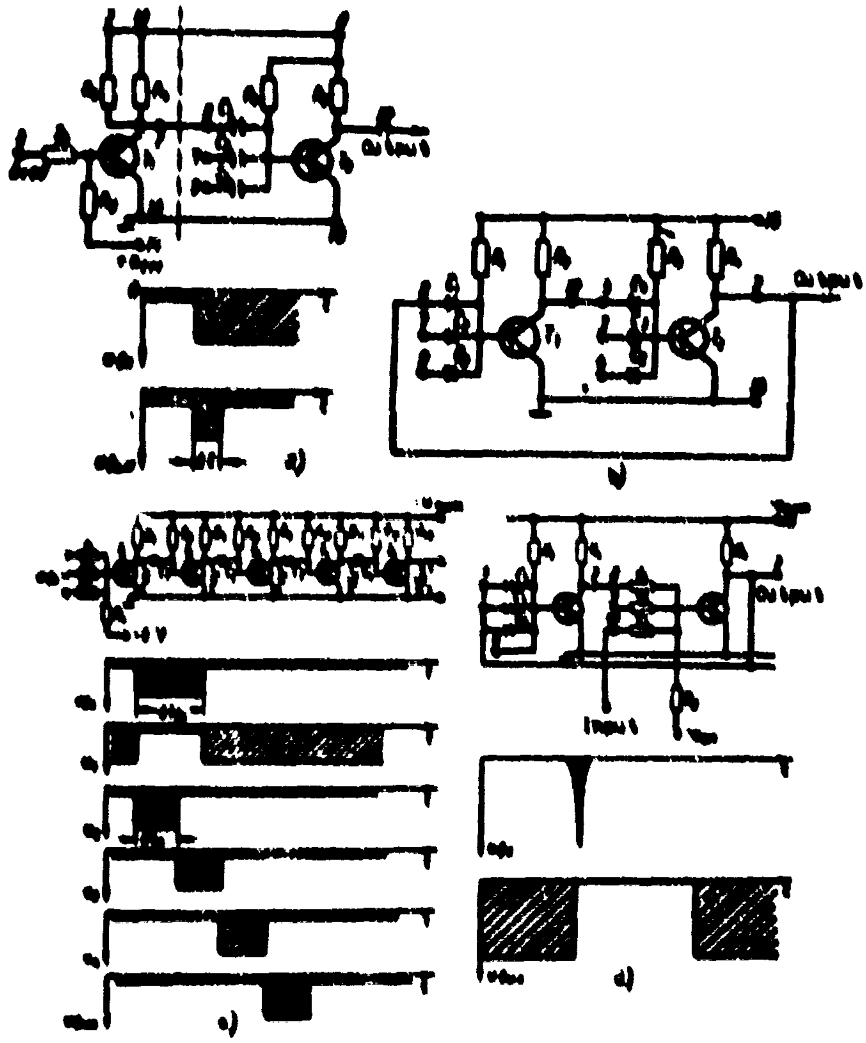


Fig. 128. Examples of application of element ET-V02 (translator delay) in circuits of automatics and telemechanics; a) limitations of the duration of signal on elements ET-L01, ET-V02; b) in circuits of multivibrators on ET-V02; c) in circuits of delay lines - application of stage connection of delay line.

In the absence of input signals in the circuit in Fig. 128a translator T_2 is saturated with base current flowing through resistor R_1. The element can operate only if capacitor C_1, (C_2 or C_3) is charged by voltage $u_{HOM} \approx E_K$ (the potential t the base of the translator is close to zero).

The supplying of input signal to the "OR-NOT" element leads to the saturation of translator T_1. To the base of translator T_2 through

capacitance C_1 (C_2 or C_3) there proceeds positive voltage, which shifts transistor T_2 to the cutoff mode. At the output there appears voltage which exists only that time during which capacitance C_1 is discharged to zero through resistor R_1 to the power supply. Then the capacitance starts to be charged by the voltage of reverse polarity via resistor R_1 from the minus of the power supply.

Upon the rising of the voltage at the capacitor to 0.1 V transistor T_2 is saturated, and the output signal disappears (Fig. 128a).

The time of the pulse width of the output voltage is determined practically only by parameters R_1C (where $C = C_1$, C_2 or C_3) and does not depend on changes of supply voltage:

$$\Delta t = 0.7R_1C.$$

In the circuit provision is made for the possibility of setting certain values of output pulse width which is assigned by selection of the corresponding capacitance C_1, C_2, C_3 or their combinations (Fig. 128b).

In systems of automatics and especially telemechanics it is often necessary to coordinate with respect to time pulse signals taken from various system elements. Certain signals have to be delayed a certain time relative to others. The signal can be delayed for the assigned time with the help of a delay line which is a series connection of several ET-V02 elements (Fig. 128c).

The voltage available at the "OR-NOT" input in the absence of an input signal ensures the charge of capacitance C_1.

The supplying of signal to the "OR-NOT" input causes saturation of transistor T_1. Transistor T_2 goes to the cutoff mode. In this case capacitance C_2 is charged, and with the disappearance of signal at the output of transistor T_2 there is ensured the cutoff mode for transistor T_3, etc.

For normal work of the delay line capacitance C_2 must succeed in being charged before the signal at the output of translator T_2 disappears, for which the resistance in the collector circuit is taken as 4 times less than the resistance of the base circuit $R_2 = R_4 = 2.4$ kΩ, $R_1 = R_3 = 10$ kΩ.

The second condition for normal work of the delay line is that, the duration of the input signal be greater than the delay of one step.

Delay element ET-V02 in conjunction with element ET-L01 makes it possible to fulfill the circuit of the kipp oscillator (Fig. 128d).

Element ET-V02 contains time-setting capacitances which can provide the following delays: 70, 300, and 700 μs.

The base lead 6 of ET-V02 can be connected to any external capacitance, which permits obtaining a wider range of change of delay.

The output element of ET-V02 can be connected to the input 8 of ET-L01 with an input impedance of 1.5 kΩ, and the level of the output must be not less than 4.5 V.

c) Element ET-V03

Element ET-V03 (Fig. 129) ensures the appearance of an output signal with delay for the time Δt after the input signal supplied to one of the inputs (leads 7, 8, and 9). The signal at the output disappears simultaneously with the disappearance of the input signal.

The parameters of element ET-V03

Supply voltage in V	+6, -12
Consumed current in mA	20
Range of regulation of time delay in s	0.5-10
Time of preparedness for repeated action in s	≥0.5
Charge resistance in kΩ	150

Utilization factor of capacitance in µF/s	7
Input impedance in kΩ	1.5
Load resistance in kΩ	0.82
Current of external load (maximum) in mA	15
Level of voltages in V:	
input signal 0 with three connected inputs	0.5
input signal 0 with one connected input	1.0

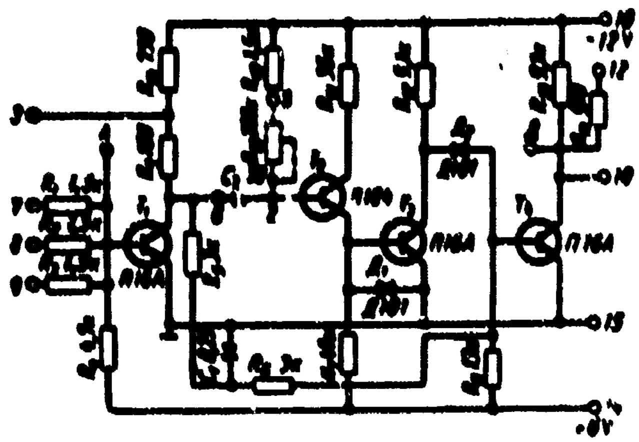


Fig. 129. The electrical schematic diagram of the time element up to 10 s (element ET-V03).

The circuit collected on transistor T_4, is a rheostat amplifier having two inputs. The first input circuit includes the collector of transistor T_1, resistors R_5 and R_6, and the base of transistor T_4; the second input circuit includes the collector of transistor T_3, diode $Д_2$, and the base of transistor T_4. The signal at the output of the element appears in the absence of signals at both inputs, i.e., when transistors T_1 and T_3 are simultaneously saturated.

The time delay can be regulated within the limits from 0.5 to 10 s by way of change of the time constant of circuit R_B with the help of resistor R_{15}, where $R_B = R_{10} + R_{15}$.

To increase the stability of the operating time of the element there is used the principle of recharging the preliminarily charged capacitance C_2 through resistors R_{10} and R_{15}.

In the absence of input signal the voltage on the collector of transistor T_1 is close to the supply voltage since $R_5 + R_6 \gg R_{16} + R_9$ (T_4 is in conditions of saturation). The voltage of the base of transistor T_2 is close to zero since transistor T_2 is saturated, and the voltage drop at the emitter-base junction is small.

In this case the voltage on the capacitor plates is close to the supply voltage. The potential of point 2 is positive relative to the potential of point 6).

Transistors T_2 and T_3 fulfill the function of a compound triode, which increases the amplification factor. If transistor T_2 is saturated, transistor T_3 is saturated; if transistor T_2 is closed, transistor T_3 is closed.

When signal is supplied to one of the inputs (leads 7, 8, and 9) transistor T_1 passes into conditions of saturation. The potential of point 6 takes zero value, the potential of point 2 takes a positive value, and transistors T_2 and T_3 are closed. The potential of the collector of transistor T_3 takes negative value, and through diode $Д_2$ transistor T_4 is kept in the saturated state after removal of negative signal via the circuit: collector of transistor T_1, resistors R_5 and R_6 and the base of transistor T_4. So that the removal of negative signal does not get ahead of appearance of negative signal in the circuit collector T_3, diode $Д_2$, base T_4, there is used delay circuit R_5, C_1R_6.

The conditions of cutoff of transistors T_2 and T_3 are ensured during the time before capacitance C_2 has been discharged to zero through resistors R_{10} and R_{15}. Then the capacitance starts to be charged by voltage of reverse polarity. During the building up of voltage on the capacitor to 0.1 V there occurs saturation of transistors T_2 and T_3. With the saturation of transistor T_3, negative signal is taken from the base of transistor T_4, and transistor T_4 is locked. On output there appears a signal delayed for the time $\Delta t = 0.7\ R_B C_2$.

During removal of input signal transistor T_1 is locked. The potential of point 6 takes negative value, point 3 positive, and transistors T_2 and T_3 are locked. Transistor T_4 passes into saturation, and the signal at the output disappears.

If the input signal disappears before the time delay has passed, the signal will not appear at the output.

After removal of the signal from the input of the element, the capacitor is recharged through resistors R_9 and R_{16}, which is determined by the time $\Delta t = 0.7 R_a C_2$, where $R_a = R_9 + R_{16}$.

After the charge of capacitance C_2 the element is ready for new action. For correct work of the element the repeated signal can be supplied to the input not earlier than in the time $\Delta t_3 = 3R_a C_2 = 0.5$ s. Otherwise the delay will be less than assigned.

Resistors $R_{15} = 200$ kΩ and capacitor $C_2 = 30$ μF are not set in the element.

When element ET-V03 is working with circuits ET-L01 it is necessary to connect leads 12 and 16. During work with circuits "AND" (on element ET-L02) leads 12 and 16 are not connected.

d) Element ET-V04

Element ET-V04 (Fig. 130) is intended for production of large signal delays with respect to time. Such time delays could be obtained in the circuit in Fig. 130 with considerable increase in capacitance C_2, which is practically unacceptable.

In element ET-V04 there is used the principle of recharging preliminarily charged capacitance C_1 through high-resistance resistor $R_B = R_7 + R_8$, having a value of sereral MΩ.

This is possible thanks to the fact that for exclusion of the influences of the resistance of the base-collector junction of transistor T_2 in its base circuit there is included a silicon

stabilitron $_1$ working in diode conditions. Instead of it there can be included a silicon diode with small reverse current (reverse resistance of 20-50 MΩ), which permits using a charge resistance of 1-2 mΩ.

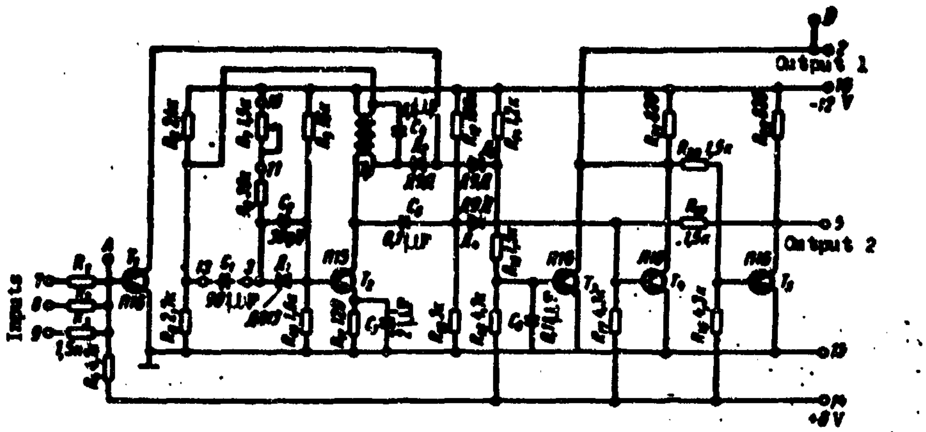


Fig. 130. Electrical schematic diagram of time element up to 100 s (element ET-V04) (capacitor C_1 and resistor R_1 are set outside the element).

For reliable fixation of the moment of change of polarity of the voltage on capacitor C_1 with slowly changing voltage on it there is used a blocking-generator consisting of transistor T_2.

The parameters of element ET-V04

Supply voltage in V	-12
Consumed current in mA	30
Range of regulation of delay in s	9-100
Time of readiness for repeated action in s	≤5
Charge resistance in kΩ	1500
Utilization factor of capacitance in μF/s	1
Input impedance in kΩ	1.50
Load resistance in kΩ	0.82
Current of external load in mA:	
nominal	10
maximum	20
Levels of voltages in V	
input signal 0 when there are three connected inputs	0.5
input signal 0 when there is one connected input	1.0

Let us examine the work of the circuit.

In the initial state of the circuit transistor T_1 is closed, capacitance C_1 is charged to the supply voltage, and transistors T_2 and T_3 are opened by constant negative bias.

As a result the flip-flop consisting of transistors T_4 and T_5 is held open by transistor T_3 in state 0, and the blocking-generator is not excited since the feedback circuit is broken by closed diode $Д_2$.

During the supplying of input signal transistor T_1 is opened, and current flows through diodes $Д_2$ and $Д_3$. The left plate of capacitor C_1 obtains zero potential, and the positive potential of the right plate closes diode $Д_1$, as a result of which the current of the base of transistor T_2 decreases and the transistor is closed. Capacitor C_1 starts to be recharged, and at the time when the potential of the right plate becomes more negative than the potential of the base of transistor T_2, diode $Д_1$ is opened, and the current in the capacitor circuit increases. As a result of the blocking-process at the output of transistor T_2 there appears a positive pulse, which passing through circuit C_5, $Д_4$, flips the flip-flop to state 1. Since transistor T_3 is closed, a signal appears at output 1 (lead 2).

The disapperance of input signal leads to locking of transistor T_1, which causes saturation of transistor T_2 and T_3, where the latter returns the flip-flop to its initial state 0.

The inverse output signal can be taken from output 2 (lead 5).

F. Amplifiers

The amplifiers ensure transmission of instructions from the elements to the actuating mechanisms. The types of amplifiers (in order of increasing power) are ET-U01, ET-U02, ET-U03, ET-U04, and ET-U05. The corresponding working currents are 0.04a, 0.125a, 0.42a, 1.25a, and 4.2a (at a maximum voltage of 24 V).

For convenience of construction of contactless control systems the input parameters of amplifiers ET-U03, ET-U04, and ET-U05 completely correspond to the output parameters of the logic elements (1.5 kΩ).

When a 1 V signal of the load circuit is supplied to any of the amplifier inputs, current flows. Thus, the output amplifier carries out the "OR" function.

$$y = a_1 \vee a_2 \vee a_3.$$

During work to an inductive load into the circuits of amplifiers there is introduced a shunting circuit $R_{Ш}$, $D_{Ш}$ connected in parallel to the load. As in known, such a circuit at a resistance of $R_{Ш} = 0$ completely excludes increase of voltage at the collector of the output transistor while the amplifier is locked but considerably increases the tripping time of the load, which is determined by the parameters of the load.

a) Element ET-U01

Element ET-U01 (the coordination amplifier) is intended for increasing the load capacities of logic circuits, for switching on signal tubes, etc.

The parameters of element ET-U01

Supply voltage in V	+6, -12
Current of load in mA:	
in normal rating	30
in conditions of raised power	40
Working frequency of inclusions in kHz	5
Value of input impedance in kΩ:	
in normal rating	0.75
in conditions of raised power	0.10

Levels of input voltage in V:	
signal 0 during work in normal rating....................	0-0.75
signal 0 during work in conditions of raised power.......	0-0.55
signal 1 during work in normal rating....................	4.0-10.2
signal 1 during work in conditions of raised power.......	1.5
Output voltage 0 in V....................................	0.15

In element ET-U01 there are constructively united two circuits of amplifiers. Each of the amplifiers has one 750 Ω input, one diode input, and one inverse output.

The diagram of the element is depicted in Fig. 131.

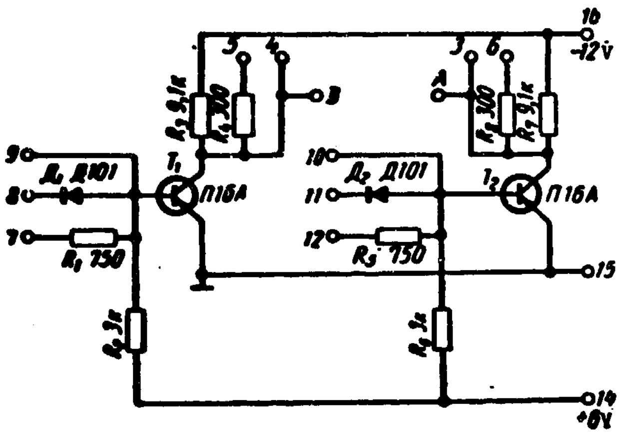


Fig. 131. The electrical schematic diagram of the coordination amplifier on a 50 mA load current (element ET-U01).

The diode input is used to increase the load current up to 40-50 mA. The input impedance of the amplifier is low when the diode input is on, which permits increasing the input current and the load current, but excludes the possibility of coordination with the output parameters of other elements.

During the work of the amplifier to the inputs of the "AND" circuit (ET-L02), in the collector circuit there are used 9.1 kΩ resistors R_3 and R_7. In all remaining cases leads 5 and 6 are united with lead 16.

b) Element ET-U02

In element ET-U02 (output amplifier) there are constructively united two circuits of amplifiers, each of which consists of one transistor included in a circuit with a common emitter (Fig. 132), and ensures the obtaining of up to 3 power at a current of up to 125 mA

The parameters of element ET-U02

Supply voltage in V	+6, -12
Current of load in mA	
in normal rating	70
in conditions of raised power	100
Working frequency of inclusion in kHz	0.5
Value of input impedance in kΩ	
in normal rating	0.75
in conditions of raised power	0.10
Levels of input voltage in V	
signal 0 during work in normal rating	0-0.75
signal 0 during work in conditions of raised power	0-0.50
signal 1 during work in normal rating	4.0-12.0
signal 1 during work in conditions of raised power	1.5
Output voltage 0 in V	0.5

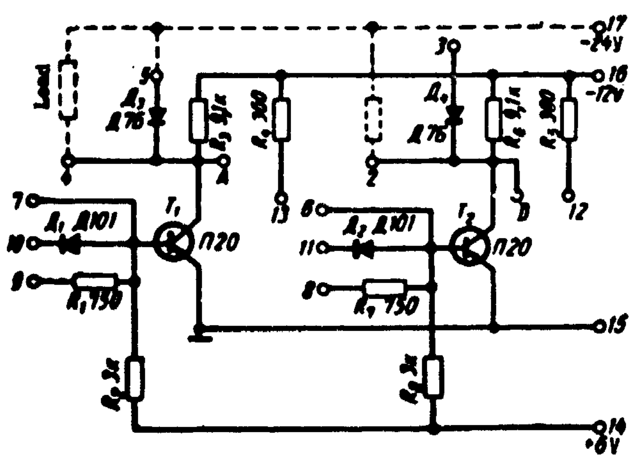


Fig. 132. The electrical schematic diagram of the output of an amplifier up to 3 at 125 mA current (element ET-U02).

During the use of ET-U02 as a coordination amplifier it is necessary to supply power from -12 V, introduce resistance R_4 = 300 Ω into the collector circuit, having connected leads 4 and 13, connect the load to lead 4, and use lead 9 through R_1 = 750 Ω as input. The current of the collector must not exceed 60-80 mA.

To increase the load current to 125 mA the input signal must be supplied through diode $Д_1$, which will allow ensuring reliable opening of triode T_1.

When the "AND" diode circuit (ET-L02) is connected to the output of the coordination amplifier, only resistor R_4 = 9.1 kΩ is used in the collector circuit.

For the work of the element to the controlled devices there is -24 V power. During work to an inductive load there is used diode $Д_3$, for which it is necessary to connect lead 5 with a -24 V bus.

In Fig. 132 the dotted line shows the rule of inclusion of a load of active and inductive character.

c) Element ET-U03

Element ET-U03 (output amplifier, Fig. 133) ensures the obtaining of power of up to 10 W at a current of 0.42a.

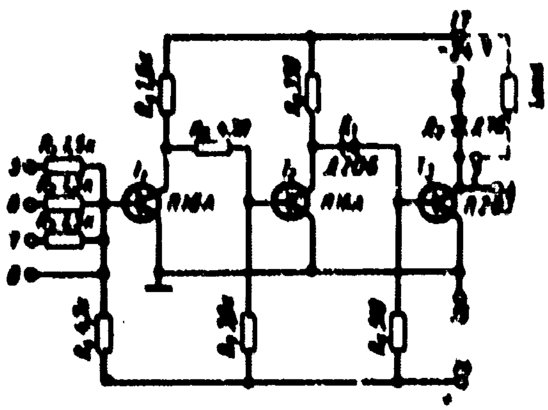


Fig. 133. The electrical schematic diagram of element ET-U03.

The output amplifier is a three-stage circuit in which all transistors are on a circuit with a common emitter.

The ET-U03 can also work with an inductive load.

The parameters of element ET-U03 are given in Table 70.

Table 70.

Type of element	Parameters		
	[illegible]	[illegible]	[illegible]
Supply voltage in V	+6 and -24	+6 and -24	+[illegible]-24
Rated power of load in W	10	[illegible]	100
Value of input impedance in k[illegible]	1,5	1,5	1,5
Levels of input voltage in V:			
signal 0 when there are three inputs	0,5	0,5	0,5
signal 0 when there is one input	1,0	1,0	1,0
signal 1	3,0–12	3,0–12	3,0–12
Limiting frequency of inclusions in Hz	1,0	1,0	1,0
Rated current of load in A	0,42	[illegible]	[illegible]
Minimum current of load in A	0,007	0,012	0,10
Minimum resistance of load in Ω	57	[illegible]	5,7
Permissible inductance of load in H	—	[illegible]	[illegible]
Consumption of current in mA	[illegible]	100	100

d) Element ET-U04

Element ET-U04 (output amplifier, Fig. 134) ensures the obtaining of power of up to 30 W at a maximum current of up to 1.25a.

The output amplifier is a four-stage circuit in which the first two transistors T_1 and T_2 are on the circuit with the common emitter, and the second two output transistors T_3 and T_4 are on the circuit of the compound transistor.

In this connection the maximum permissible current of diode $Д_ш$ is less than the current of the load, and during frequency cutoffs there is possible overload of the diode with respect to current.

In this case the external wiring must be connected to additional shunting diode $Д_ш$.

The parameters of element ET-U04 are given in Table 70.

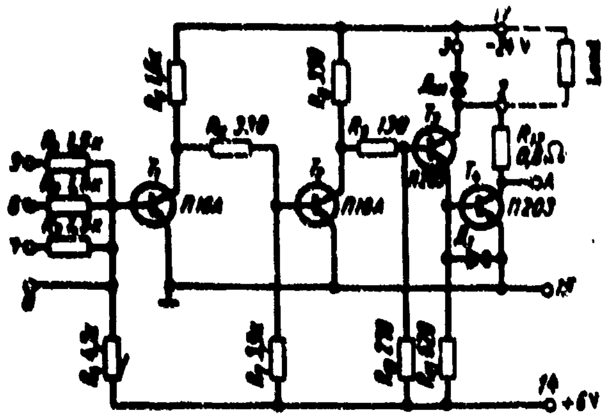


Fig. 134. Schematic diagram of element ET-U04.

e) Element ET-U05

Element ET-U05 (output amplifier, Fig. 135) ensures obtaining of power of up to 100 W at maximum current of up to 4.2a.

The layout of element ET-U05 is analogous to the layout of element ET-U04.

The coupling between the pre-exit transistor T_2 and the output compound transistor is carried out wi'' e help of two diodes $Д_1$ and $Д_2$.

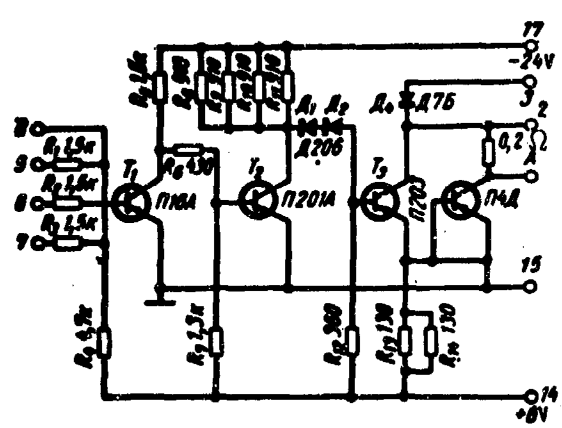


Fig. 135. The schematic diagram of element ET-U05.

The application of two diodes in the coupling between stages is caused by the need to have a $u_{\text{зап}}$ of the compound tri le of about 1 V, which cannot be obtained on one diode. The parameters of element ET-U05 are given in Table 70.

G. Power Supplies

Element ET is powered by standardized power units. There are 5 performances of blocks: three units stabilized — on 20, 100, and 500 W — and two units unstabilized — on 160 and 500 W.

Logic and functional elements are powered from stabilized blocks; output devices from unstabilized blocks.

Stabilized power units are not intended for loads subject to sharp changes. Unstabilized feed units, conversely, allow simultaneous switching on and switching off of hundred-percent load.

The power units, with the exception of the 20 W stabilized unit, each have three circuits of rectified voltages connected by a common (zero) wire: +6 V; -12 V and -25 V. The 20 W block has only two loops: +6 V and -12 V.

In stabilized power units 25 V circuits are auxiliary and are not stabilized.

To increase the reliability of work for stabilized power units there were accepted circuits with magnetic amplifiers.

Stabilized power supplies with regulating magnetic amplifiers (MU) possess high enough internal resistance (inductive); therefore, they do not fear short circuits on output terminals. So that during short circuit in one circuit, voltage is taken to another circuit (practically lowered a few times), at the output of both circuits there are set voltage relays which by their contacts connect the locking winding to the MU of both circuits. In a short-circuited circuit the current is lowered to a very low value, and in an unimpaired circuit the voltage falls to 0.1-0.2 nominal value.

Stabilized power units ensure the possibility of short-term (not more than 30 min) simultaneous lowering of voltage at the output terminals of the circuits from +6 and -12 V to 75% of nominal value. Stabilization of units is absent. Switching to a lower voltage is carried out with the help of toggle switches.

All power units are equipped with shielding excluding the going out of order of the unit during energency conditions in the load circuits.

Electrical connection of power units with external circuits is carried out with the help of plug connectors, each circuit having two contacts for the purpose of duplicating and increasing the realiability of the connections.

The technical data of the power units are given in Table 71.

Table 71. Technical data of power units.

Type of unit	Rated power of all output circuits on the side of the rectified current in W	Kind of current and feed voltage in V	Voltage and power of output circuits on the side of direct current	Permissible multiplicity of change of load current	Permissible level of pulsations of output voltage	Permissible change of mean value of output voltage in +6 and -12 V circuits in %
ЭТ-П20С	20	Single-phase 220	+6 V; —12 V; 4 W; 16 W	10	3	±2
ЭТ-П100С	100	Single-phase 220	26 V; —12 V; —25 V; 18 W 72 W; 10 W	5	3	±2
ЭТ-П500С	500	Three-phase 220/380	+6 V; —12 V; —25 V; 80 W; 400 W; 20 W;	3	3	±2
ЭТ-П100	100	Three-phase 220/380	+6 V; —12 V; —25 V; 15 W; 40 W; 105 W	—	6.5	—
ЭТ-П500	500	Three-phase 220/380	+6 V; —12 V; —25 V; 30 W; 80 W; 410 W	—	6.5	—

Note: All face values of resistances and capacitors given in the diagrams can be modified.

3. Application of Elements of the ET Series in Industrial Automatics

When ET series elements are used, the following must be kept in mind.

1. The elements have relay equivalents. In the case of a smoothly varing input signal (from the temperature sensor, the pressure sensor, etc.,) it is necessary to convert it into a discrete signal of the established level with the help of an ET-F02 element or an ET-F03 null-balance device.

2. Logic operations are realized by a combination of elements.

Realization of basic logic dependences on ET is represented in Table 72. Realization of certain time operations is represented in Table 73. Application of ET series elements in calculating subassemblies of systems is examined in Table 74.

Table 72. Examples of application of the elements of the ET series for realization of basic logic operations.

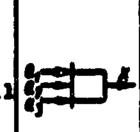
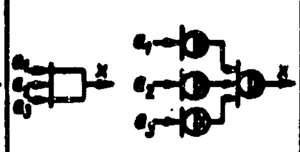
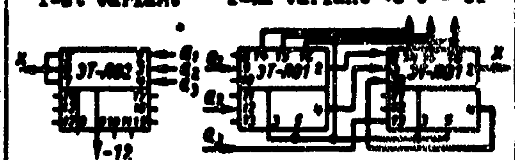
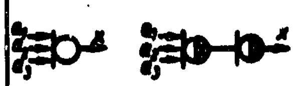
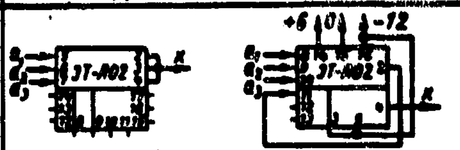
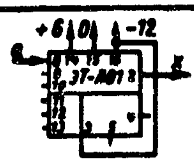
No.	Designation and description of logic operations	Graphic representation in block diagrams	Circuit realizing function with the help of ET element	Representation in wiring diagrams
1	Operation "AND" Signal appear at output when there are signals at all inputs.			1-st variant 2-nd variant +6 0 - 12 
2	"OR" operation Signal appears at output when there is a signal at at least one of the inputs.			
3	"NOT" operation In the presence of a signal at the input the signal at the output is absent. The signal at the output appears when the signal at the input disappears.			

Table 72. (cont'd).

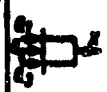
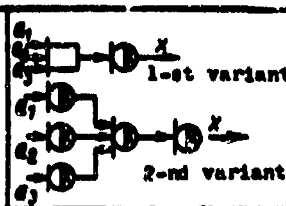
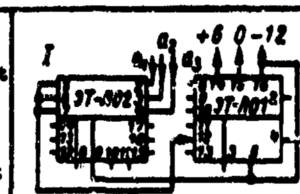
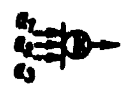
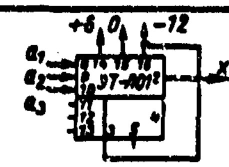
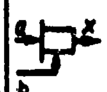
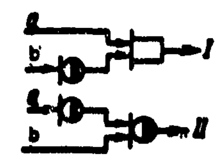
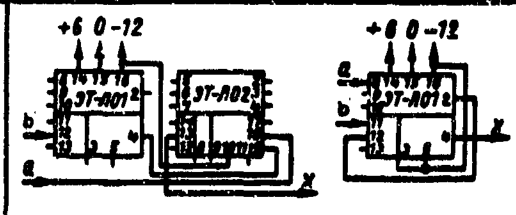
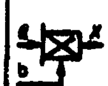
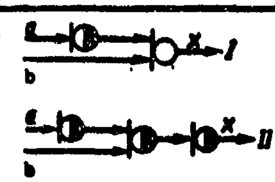
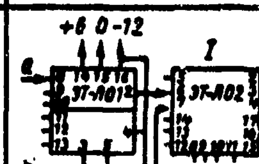
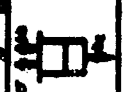
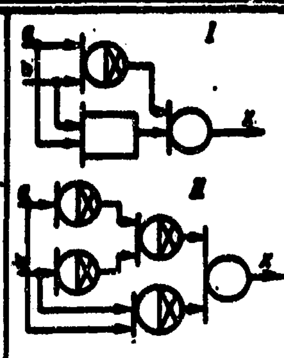
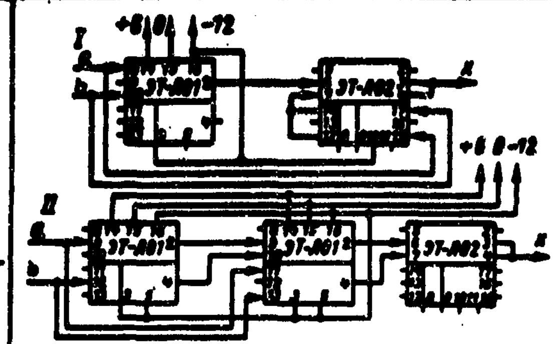
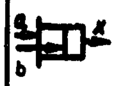
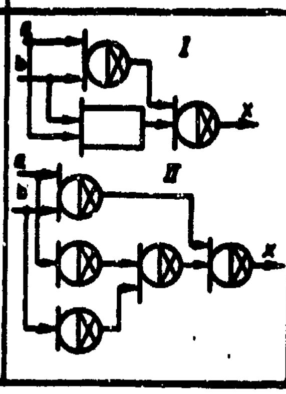
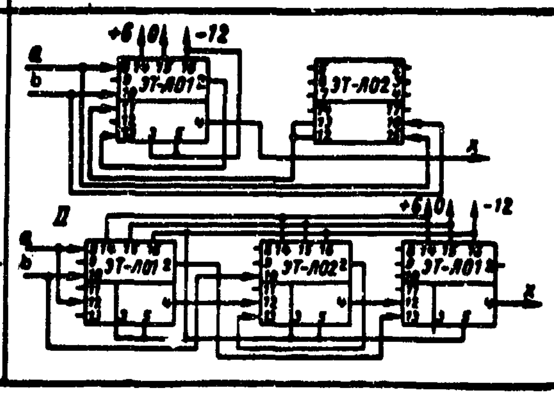
4	Schaffer "AND-NOT" operation. The signal at the output is absent when there are signals at all three inputs.			 The 2-nd variant is examined in Fig. 113g, page 53
5	The Pierce "OR-NOT" operation. The signal is absent at output, when there is a signal at at least one of the three inputs.			
6	Ban. In the absence of signal at the inhibition input "b" the signal at the output appears simultaneously with the signal at input "a"; in the presence of a signal is absent at the output.			
7	Implication. The signal is absent at the output if and only if there is a signal at input "a" and the signal at input "b" is absent.			 The 2-nd variant is examined in Fig. 1131, page 53
8	Equivalence (equivalentness) The signal at the output exists if and only if at both inputs simultaneously there are or are absent input signals.			
9	Unequivalence (unequivalentness) A signal exists at the output if and only if the signals at inputs "a" and "b" do not coincide.			

Table 72. (cont'd).

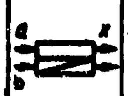
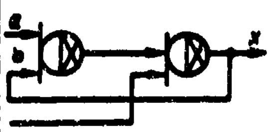
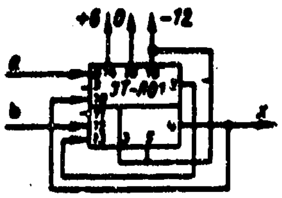
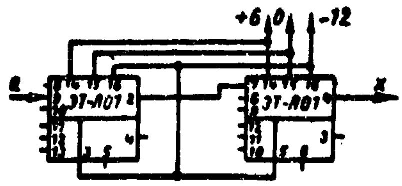
10	"Memory" After a signal is supplied to the input "a" of switching on of memory there appears a signal at the forward output and it disappears at the inverse output. This state is preserved until a signal is supplied to the input "b" of switching off of memory. After the supplying of power the state of the circuit is arbitrary.			
11	"Repetition" Amplification of the input signal with preservation of its sign.			

Table 73. Examples of using ET elements to realize certain time operations.

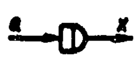
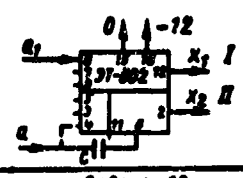
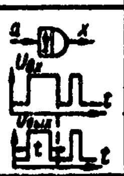
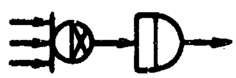
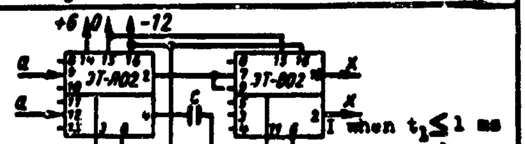
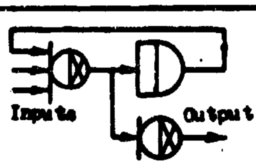
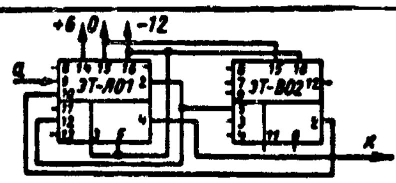
No. in order	Designation and description of time operations	Representation in block diagrams and time diagrams of work	Circuit realizing time operation on ET elements	Representation in wiring diagrams
1	Formation of output pulse of assigned width. The signal at the output appears simultaneously with the disappearance of the signal at the input and exists t_1 s.			 At $t_1 \geq 1$ ms there is established the external capacitance
2	Time of presence of signal. The signal at the output appears simultaneously with the signal at the input and exists t s.			 I when $t_1 \leq 1$ ms II when $t_1 \geq 1$ ms
3	Expansion of input pulse (kipp oscillator). The signal at the output appears simultaneously with the signal at the input and exists t s			

Table 73. (cont'd).

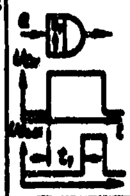
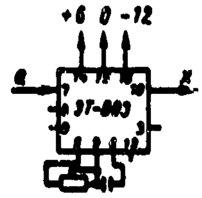
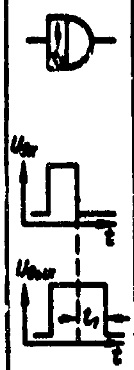
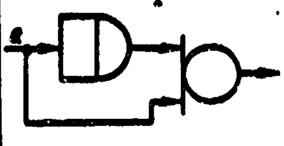
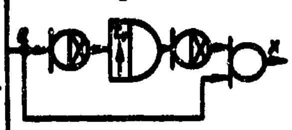
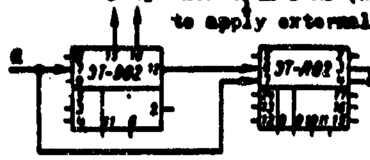
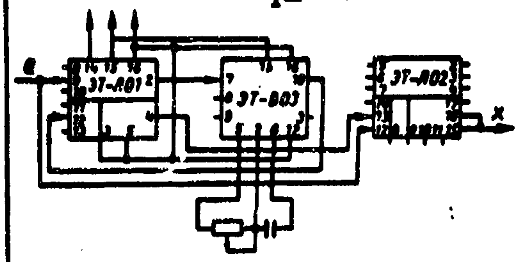
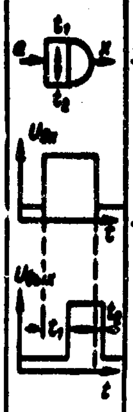
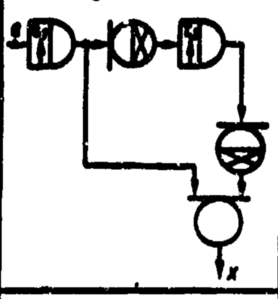
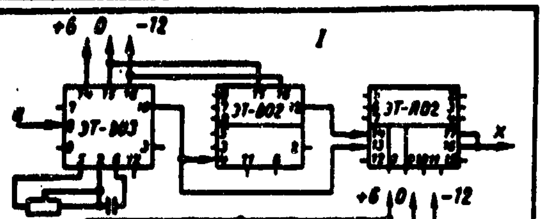
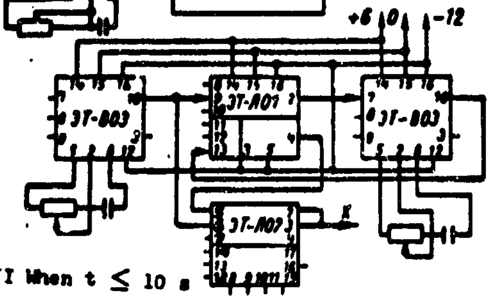
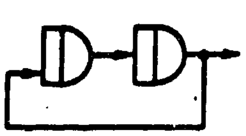
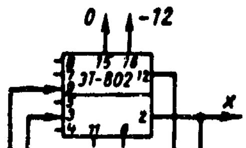
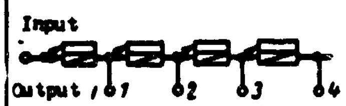
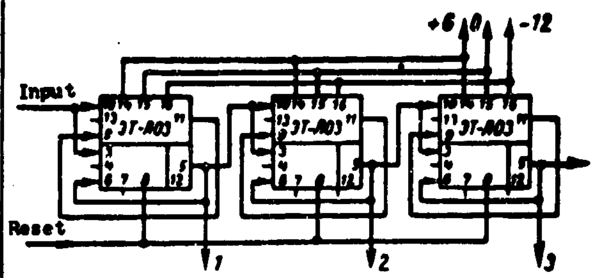
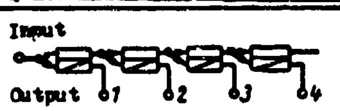
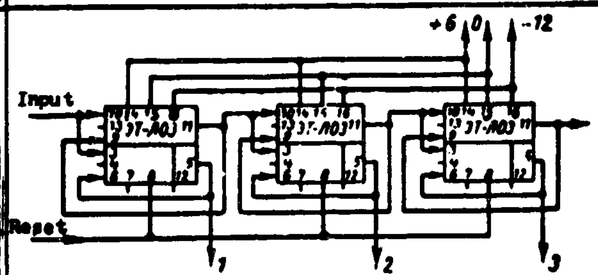
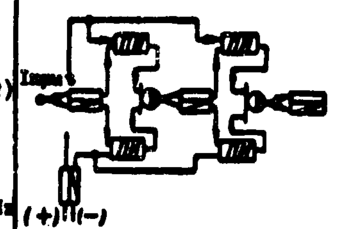
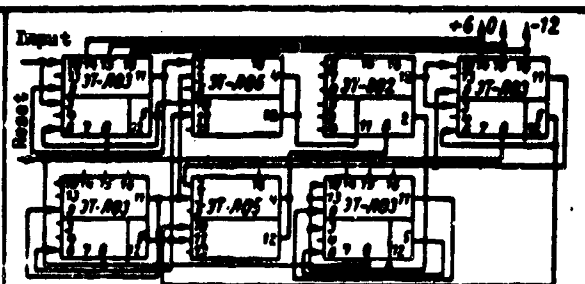
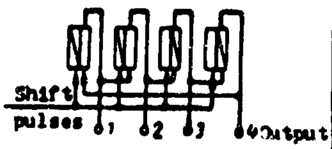
4	Delay of appearance of signal. The signal at the output appears t_1 s after the supplying of a signal to the input disappears simultaneously with the signal at the input.			
5	Delay of the disappearance of the signal. The signal at the output appears simultaneously with the signal at the input, and the signal at the output disappears t_1 s after the disappearance of the signal at the input.		When $t_1 \leq 0.1$ s  When $t_1 \leq 10$ s 	When $t_1 \leq 1$ ms (when $t \geq 1$ ms to apply external capacitance)  When $t_1 \leq 10$ s 
6	Delay of appearance and delay of disappearance of signal. The signal at the output appears t_1 s after the signal is supplied to the input and disappears t_2 s after the disappearance of the input signal.		When $t_2 \leq 0.1$ s I  When $t_2 \leq 10$ s II 	I   II When $t \leq 10$ s
7	Pulsing (multivibrator).			

Table 74. Examples of application of ET elements in calculating subassemblies of the system.

<table>
<tr><th>No. in order</th><th>Diagram of work and structural diagram of subassembly</th><th>Designation and function of subassembly</th><th>Representation in wiring diagrams</th></tr>
<tr><td>1</td><td>Binary integrating counter. Adding of pulse entering the input with the number recorded earlier in the counter and delivery of the result in binary code. Frequency of input pulses – up to 5 kHz.</td><td>

<table>
<tr><th>Outputs</th><th>1</th><th>2</th><th>3</th><th>4</th></tr>
<tr><td>Initial position</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>After the 1-st pulse</td><td>1</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>After the 2-nd pulse</td><td>0</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>After the 14-th pulse</td><td>0</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>After the 15-th pulse</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>After the 16-th pulse</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
</table></td><td>
</td></tr>
<tr><td>2</td><td>Binary subtracting counter. Subtraction of pulses entering the input from the number recorded earlier in the counter. Frequency of input pulses – up to 5 kHz.</td><td>

<table>
<tr><th>Outputs</th><th>1</th><th>2</th><th>3</th><th>4</th></tr>
<tr><td>Initial position</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>After the 1-st pulse</td><td>0</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>After the 2-nd pulse</td><td>1</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>After the 15-th pulse</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>After the 16-th pulse</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
</table></td><td>
</td></tr>
<tr><td>3</td><td>Binary reversible counter. Addition (1) or subtraction (2) of input pulses in accordance with the last instruction. Frequency of input pulses – up to 1.5 kHz</td><td>
</td><td>
</td></tr>
<tr><td>4</td><td>Shifting register. Shifting of the number recorded earlier in the register one position by every shift pulse. In the special case-annular switch. Frequency of input pulses up to 1.5 kHz.</td><td>

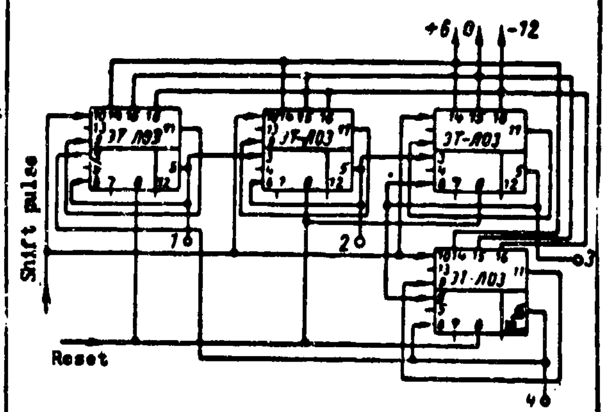
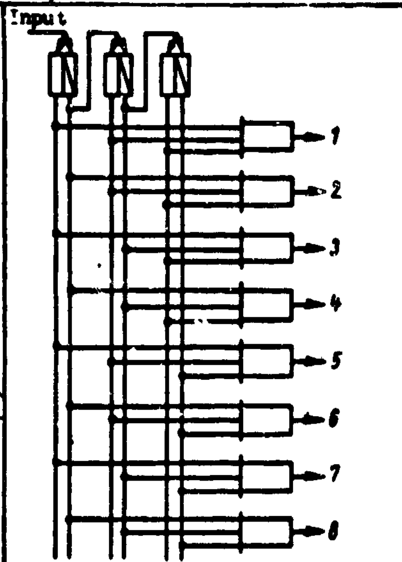
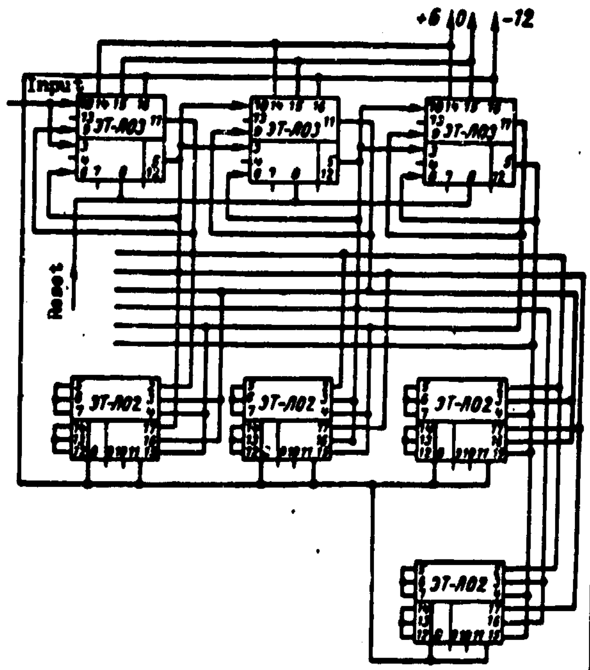
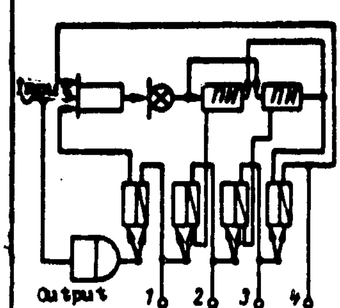
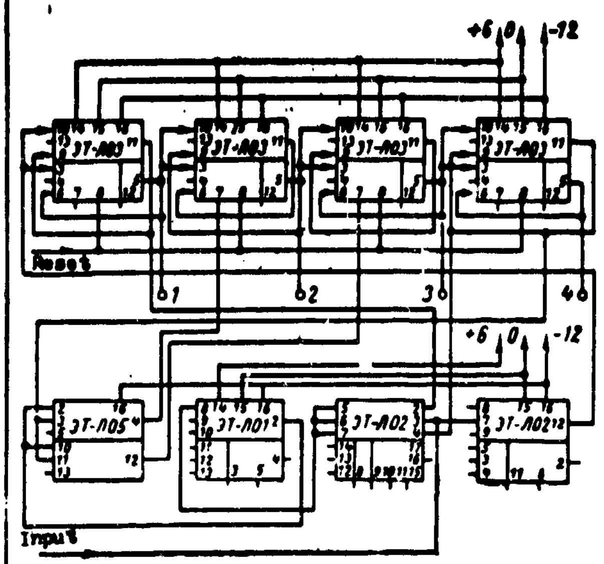
<table>
<tr><th>Outputs</th><th>1</th><th>2</th><th>3</th><th>4</th></tr>
<tr><td>Initial position</td><td>1</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>After 1-st pulse</td><td>0</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>After 2-nd pulse</td><td>0</td><td>0</td><td>1</td><td>1</td></tr>
</table>
<table>
<tr><th>Outputs</th><th>1</th><th>2</th><th>3</th><th>4</th></tr>
<tr><td>Initial position</td><td>1</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>After 1-st pulse</td><td>0</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>After 2-nd pulse</td><td>0</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>After 3-rd pulse</td><td>0</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>After 4-th pulse</td><td>1</td><td>0</td><td>0</td><td>0</td></tr>
</table></td><td>
</td></tr>
</table>

Table 74. (cont'd).

5	Annular register (on the basis of a counter with a decoder) Series switching of signals at the output of the register when any number of input pulses are supplied. Frequency of input pulses – up to 5 kHz		
6	Binary-decimal counter. Adding of input pulses to 10 with return to the initial state after each 10-th pulse. Frequency of input pulses – up to 1.5 kHz.		

Outputs	1	2	3	4	5	6	7	8
Initial position	1	0	0	0	0	0	0	0
After 1-st pulse	0	1	0	0	0	0	0	0
After 2-nd pulse	0	0	1	0	0	0	0	0
After 7-th pulse	0	0	0	0	0	0	0	1
After 8-th pulse	1	0	0	0	0	0	0	0
After 9-th pulse	0	1	0	0	0	0	0	0

Outputs	1	2	3	4
Initial position	0	0	0	0
After 1-st pulse	1	0	0	0
After 2-nd pulse	0	1	0	0
After 8-th pulse	0	0	0	1
After 9-th pulse	1	1	1	1
After 10-th pulse	0	0	0	0

During construction of block diagrams it is recommended that the graphic representations of elements of circuits and logic functions examined in Table 75 be used.

Conditional literal designations of sensors are composed in accordance with All Union State Standard 3925-59. The graphic representation of sensors is depicted in Table 76.

Table 75. Graphic representation of logic functions in block diagrams.

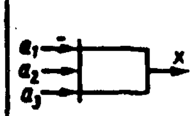
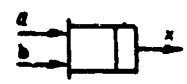
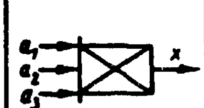
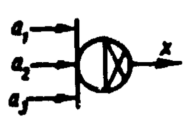
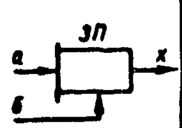
No. in order	Designation of function	Graphic representation in block diagrams	No. in order	Designation of function	Graphic representation in block diagrams
1	"AND"		7	"Implication"	
2	"OR"		8	"Equivalence" ("equivalentness")	
3	"NOT"		9	"Unequivalence" ("unequivalentness")	
4	"Schaffer" "AND-NOT"		10	"Memory"	
5	"Pierce" "OR-NOT"		11	"Repetition"	
6	"Inhibition"		12	"Memory" circuit with computing input (computing flip-flop)	

Table 76. Graphic representation of auxiliary, input, and output elements in block diagrams.

No. in order	Designation	Graphic representation in block diagrams
1	Sensors with forward output	
2	Sensors with forward and inverse output	
3	Power amplifier	
4	Repeater	

Graphic representation of time function in block diagrams.

No. in order	Designation of function	Graphic representation of function
1	Formation of output pulse of assigned width.	
2	Time of presence of signal.	
3	Expansion of input pulse (kipp oscillator).	
4	Endurance on appearance of signal.	
5	Delay of appearance of signal.	
6	Delay of appearance and delay of disappearance of signal.	

Footnotes

[1]The given complex of elements was replaced by another complex of elements the description of which is given on pp. 270-277. [Translator's Note: Pages 270-277 refer to Russian document. They have not been translated in this manuscript.]

[2]The buffer module is an additional module included in the circuit to increase the power of the output signal.